



# PY32F072 Datasheet

32-bit ARM<sup>®</sup> Cortex<sup>®</sup>-M0+ Microcontroller



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## Features

- Core
  - ARM® 32-bit Cortex®-M0+ CPU
  - Up to 72 MHz operating frequency
- Memories
  - Maximum 128 KB Flash memory
  - Maximum 16 KB SRAM
- Clock management
  - Internal 4/8/16/22.12/24 MHz high speed clock (HSI)
  - Internal 32.768 kHz low speed clock (LSI)
  - External 4 to 32 MHz high speed crystal oscillator (HSE)
  - External 32.768 kHz low-speed crystal oscillator (LSE)
  - PLL (supports 2/3 multiplication of HSI or HSE)
- Power management and reset
  - Operating voltage: 1.7 ~ 5.5 V
  - Low power modes : Sleep and Stop
  - Power-on/power-down reset (POR/PDR)
  - Brown-out reset (BOR)
  - Programmable voltage detection (PVD)
- General-purpose input and output (I/O)
  - Up to 58 I/Os, all available as external interrupts
- 7-channel DMA controller
- Two 12-bit ADC
  - Up to 16 external input channels
  - Input voltage conversion range: 0 to  $V_{CCA}$
- Two 12-bit DAC, supports 2 channels
- 3 analog comparators
- 3-channel operational amplifier
- Support 8 \* 36 / 4 \* 40 LCD
- 13 timers
  - One 16-bit advanced-control timer (TIM1)
  - One 32-bit general-purpose timer (TIM2)
  - Five 16-bit general-purpose timers (TIM3/14/15/16/17)
  - Two basic timers (TIM6/TIM7)
  - A low power timer (LPTIM)
  - A independent watchdog timer (IWDG)
  - A window watchdog timer (WWDG)
  - A SysTick timer
- RTC
- Communication interfaces
  - Two serial peripheral interfaces (SPI) with I<sup>2</sup>S function
  - Four universal synchronous/asynchronous Transceivers (USARTs) , support automatic baud rate detection, two of USARTs support ISO7816, LIN and IrDA
  - Two I<sup>2</sup>C interfaces supporting standard mode (100 kHz), Fast mode (400 kHz), 7-bit/10-bit addressing mode and SMBus
  - USB 2.0 full-speed interface
  - CAN 2.0 standard communication interface
- Hardware CRC-32 module
- Hardware 32-bit divider (DIV)
- Unique UID
- Serial wire debug (SWD)
- Operating temp: -40 ~ 85 °C, - 40 ~ 105 °C
- Package: LQFP64, LQFP48, QFN48, QFN32 (5\*5) , QFN32 (4\*4)

## Content

<b>Features</b> .....	<b>2</b>
<b>1. Introduction</b> .....	<b>6</b>
<b>2. Functional Overview</b> .....	<b>9</b>
2.1. Arm®-Cortex®-M0+ core .....	9
2.2. Memories .....	9
2.3. Boot modes .....	10
2.4. Clock system.....	10
2.5. Power management.....	12
2.5.1. Power block diagram.....	12
2.5.2. Power monitoring.....	12
2.5.3. Voltage regulator .....	13
2.5.4. Low-power mode.....	14
2.6. Reset.....	14
2.6.1. Power reset .....	14
2.6.2. System reset.....	14
2.7. General-purpose inputs and outputs (GPIOs) .....	14
2.8. Hardware divider (DIV) .....	14
2.9. Direct memory access controller (DMA) .....	15
2.10. Interrupts and events .....	15
2.10.1. Nested vectored interrupt controller (NVIC).....	16
2.10.2. Extended interrupt/event controller (EXTI).....	16
2.11. Analog-to-digital converter (ADC) .....	17
2.12. Digital-to-analog converter (DAC).....	17
2.13. Comparators (COMP) .....	17
2.14. Operational amplifier (OPA).....	18
2.15. Hardware divider (DIV).....	18
2.16. Liquid crystal display (LCD) controller .....	18
2.17. Timer .....	19
2.17.1. Advanced-control timer (TIM1).....	19
2.17.2. General-purpose timers.....	20
2.17.3. Basic timers (TIM6/TIM7) .....	21
2.17.4. Low power timer (LPTIM).....	21
2.17.5. Independent watchdog (IWDG).....	21
2.17.6. System window watchdog (WWDG) .....	21
2.17.7. SysTick timer .....	21
2.18. Real-time clock (RTC).....	22
2.19. Cyclic redundancy check cell(CRC).....	22
2.20. Clock check system (CTC).....	22
2.21. System configuration controller (SYSCFG) .....	23

2.22.	Debug support (DBG) .....	23
2.23.	Inter-integrated circuit interface (I <sup>2</sup> C) .....	23
2.24.	Universal synchronous/asynchronous receiver transmitter (USART).....	24
2.25.	Serial peripheral interface (SPI) .....	25
2.26.	USB2.0 full-speed module .....	26
2.27.	CAN .....	26
2.28.	Serial wire debug (SWD).....	27
<b>3.</b>	<b>Pin Configuration.....</b>	<b>28</b>
3.1.	PortA alternate function mapping.....	39
3.2.	PortB alternate function mapping.....	40
3.3.	PortC alternate function mapping .....	41
3.4.	PortF alternate function mapping.....	41
<b>4.</b>	<b>Memory Map.....</b>	<b>43</b>
<b>5.</b>	<b>Electrical Characteristics.....</b>	<b>47</b>
5.1.	Parameter conditions .....	47
5.1.1.	Minium and maximum values.....	47
5.1.2.	Typical values.....	47
5.2.	Absolute maximum ratings.....	47
5.3.	Operating conditions .....	48
5.3.1.	General operating conditions .....	48
5.3.2.	Operating conditions at power-up / power-down.....	48
5.3.3.	Embedded reset and PVD module features.....	48
5.3.4.	Operating current characteristics .....	49
5.3.5.	Wakeup time from low-power modes.....	51
5.3.6.	External clock source characteristics .....	51
5.3.7.	Internal high frequency clock source HSI characteristics .....	54
5.3.8.	Internal low frequency clock source LSI characteristics .....	55
5.3.9.	Phase locked loop (PLL) characteristics .....	55
5.3.10.	Memory characteristics .....	55
5.3.11.	EFT characteristics.....	56
5.3.12.	ESD & LU characteristics .....	56
5.3.13.	Port characteristics .....	56
5.3.14.	NRST pin characteristics.....	57
5.3.15.	ADC characteristics .....	57
5.3.16.	DAC characteristics .....	58
5.3.17.	Comparator characteristics .....	59
5.3.18.	Operational amplifier characteristics .....	59
5.3.19.	Temperature sensor characteristics .....	60
5.3.20.	LCD Controller Characteristics.....	60
5.3.21.	Built-in reference voltage characteristics .....	60

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5.3.22. ADC Built-in reference voltage characteristics .....	61
5.3.23. Timer characteristics .....	61
5.3.24. Communication port characteristics .....	62
<b>6. Package Information .....</b>	<b>65</b>
6.1. LQFP64 package size .....	65
6.2. LQFP48 package size .....	66
6.3. QFN48 package size .....	67
6.4. QFN32(5*5) package size .....	68
6.5. QFN32(4*4) package size .....	69
<b>7. Ordering Information .....</b>	<b>70</b>
<b>8. Version History .....</b>	<b>71</b>

# 1. Introduction

PY32F072 series microcontrollers incorporate high-performance ARM® 32-bit Cortex®-M0+ core, wide operating range voltage, embedded memories with up to 128 KB Flash and 32 KB SRAM, frequency up to 72 MHz, and contains various products in different package types. The chip integrates multi-channel I<sup>2</sup>C, SPI, USART and other communication peripherals, one 12-bit ADC, two DAC, 13 timers, one USB 2.0, one CAN 2.0, three comparators, three operational amplifiers, and one LCD driver.

PY32F072 series microcontrollers 's operate in the temperature range from -40 to 85°C or -40 to 105°C, and with operating voltages from 1.7 to 5.5 V. The chip provides sleep and stop low-power operating modes, which can meet different low-power applications.

The devices are suitable for various application scenarios, such as controllers, portable devices, PC peripherals, gaming and GPS platforms, industrial applications.

Table 1-1 PY32F072x6 series device features and peripheral counts

Peripherals		PY32F072R1BT6	PY32F072C1BT6	PY32F072C1BU6	PY32F072K1BU6
Flash memory (KB)		128	128	128	128
SRAM (KB)		16	16	16	16
Timers	Advanced	1 (16-bit)			
	General pupose	5 (16-bit)			
	Basic	1(32-bit)			
	low power	2			
	SysTick	1			
	Watchdog	2			
Comm. inter-faces	SPI[I <sup>2</sup> S]	2[2]			
	I <sup>2</sup> C	2			
	USART	4			
	CAN	1			
	USB	1			
DMA		7ch			
RTC		Yes			
GPIOs		58	42	42	28
12-bit ADC ( external + internal)		1 (16 + 8)	1 (10 + 8)	1 (10 + 8)	1 (10 + 8)
DAC (Channels)		2 (2)			
Comparators		3			
OPA		3			
LCD		1			
Max. CPU frequency		72 MHz			
Operating Voltage		1.7 - 5.5 V			
Operating Temp.		- 40 ~ 85 °C			
Package		LQFP64	LQFP48	QFN48	QFN32(5*5)

Table 1-2 PY32F072x7 series device features and peripheral counts

Peripherals		PY32F072C1BT7	PY32F072K3BU7
Flash memory (KB)		128	128
SRAM (KB)		16	16
Timers	Advanced	1 (16-bit)	
	General purpose	5 (16-bit)	
		1(32-bit)	
	Basic	2	
	low power	1	
	SysTick	1	
Watchdog	2		
Comm. interfaces	SPI[I <sup>2</sup> S]	2[2]	
	I <sup>2</sup> C	2	
	USART	4	
	CAN	1	
	USB	1	
DMA		7ch	
RTC		Yes	
GPIOs		42	28
12-bit ADC ( external + internal)		1 (10 + 8)	1 (10 + 8)
DAC (Channels)		2 (2)	2 (2)
Comparators		3	3
OPA		3	3
LCD		1	1
Max. CPU frequency		72 MHz	
Operating Voltage		1.7 - 5.5 V	
Operating Temp.		- 40 ~ 105 °C	
Package		LQFP48	QFN32(4*4)

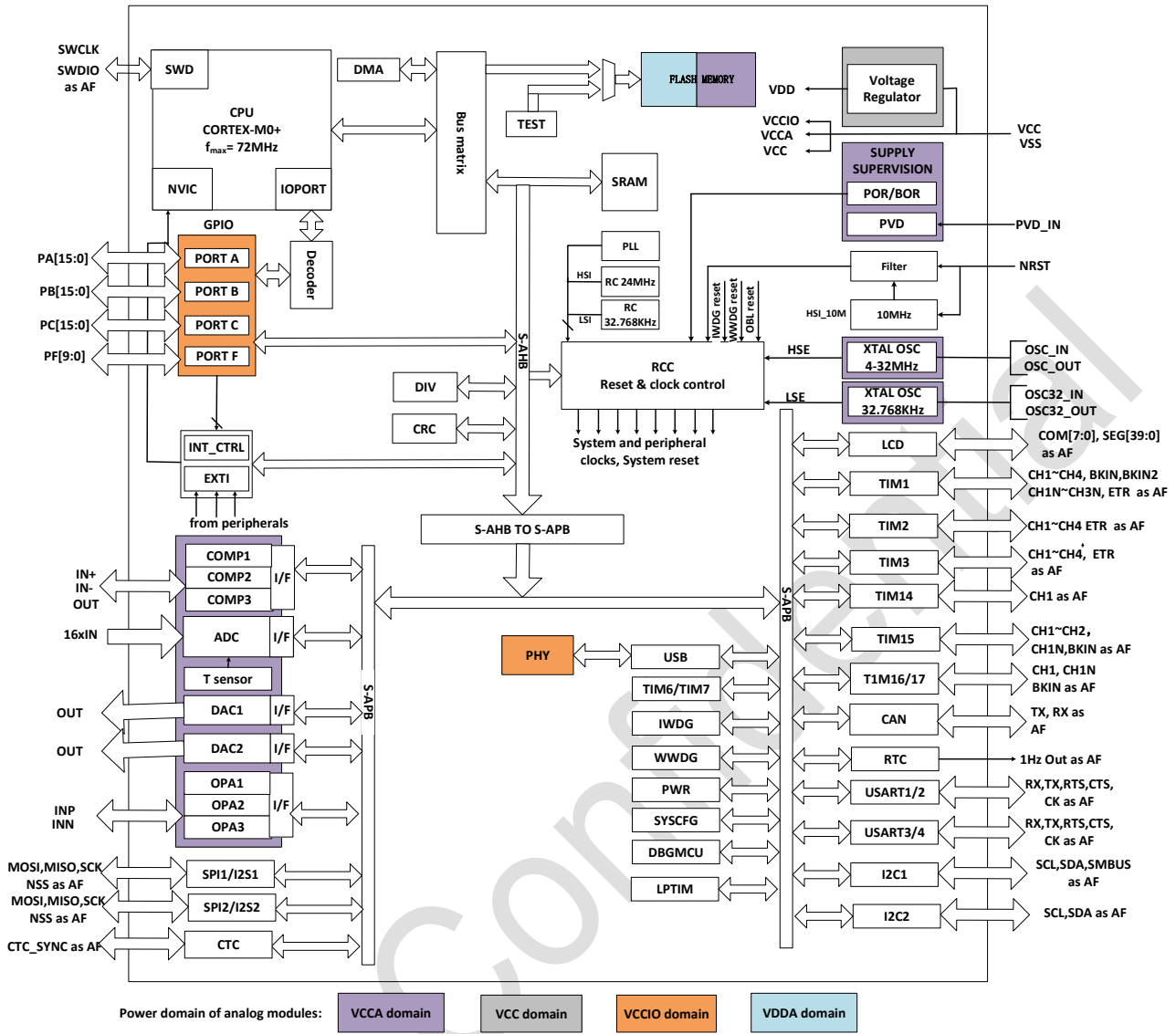


Figure 1-1 System block diagram



## 2. Functional Overview

### 2.1. Arm<sup>®</sup>-Cortex<sup>®</sup>-M0+ core

The Arm<sup>®</sup> Cortex<sup>®</sup>-M0+ is an entry-level Arm 32-bit Cortex processor designed for a wide range of embedded applications. It provides developers with significant benefits, including:

- Simple structure, easy to learn and program
- Ultra-low power consumption, energy-saving operation
- Reduced code density and more

Cortex-M0+ processor is a 32-bit core optimized for area and power consumption and is a 2-stage pipeline Von Neumann architecture. The processor offers high-end processing hardware, including single-cycle multipliers, through a streamlined but powerful instruction set and an extensively optimized design. Moreover, it delivers the superior performance expected from a 32-bit architecture computer, with a higher coding density than other 8 and 16-bit microcontrollers.

The Cortex-M0+ is tightly coupled with a Nested Vectored Interrupt Controller (NVIC).

### 2.2. Memories

The on-chip integrated SRAM is accessed by bytes (8 bits), half-word (16 bits) or word (32 bits).

The on-chip integrated Flash consists of two different physical areas:

- Main flash area contains application and user data
- Information area has 14 KB, and it includes the following parts:
  - Option bytes
  - UID bytes
  - System memory

The protection of Flash main memory includes the following mechanisms:

- Read protection (RDP) prevents outside access.
- Write protection (WRP) prevents unwanted write operation (confuse by program memory pointer from PC). The minimum protection unit for write protection is 8 KB .
- Option byte write protection is a special design for unlock.

## 2.3. Boot modes

At startup, the BOOT0 pin and boot selector option bit nBOOT are used to select one of the three boot options in the following table:

Table 2-1 Boot configuration

Boot mode configuration		Mode
nBOOT1 bit	BOOT0 pin	
X	0	Main flash as the boot area
1	1	System memory as the boot area
0	1	SRAM as the boot area

The Boot loader is located in the System memory and is used to download the Flash program through the USART interface.

## 2.4. Clock system

At startup, the default system clock frequency is HSI 8 MHz, and after the program is operating the system clock frequency and system clock source can be reconfigured. The frequency clocks that can be selected are:

- A 4/8/16/22.12/24 MHz configurable internal high precision HSI clock
- A 32.768 kHz configurable internal LSI clock
- A 4 to 32 MHz HSE clock, and used to enable the CSS function to detect HSE. If CSS fails, the hardware will automatically convert the system clock to HSI, and software configures the HSI frequency. Simultaneously, CPU NMI interrupt is generated.
- A 32.768 kHz LSE clock.
- PLL clock has HSI and HSE sources. If the HSE source is selected, when CSS is enabled and CSS fails, the PLL and HSE will be turned off, and the hardware selects the system clock source as HSI.

The AHB clock can be divided based on the system clock, and the APB clock can be divided based on the AHB clock. AHB and APB clock frequencies up to 72 MHz.

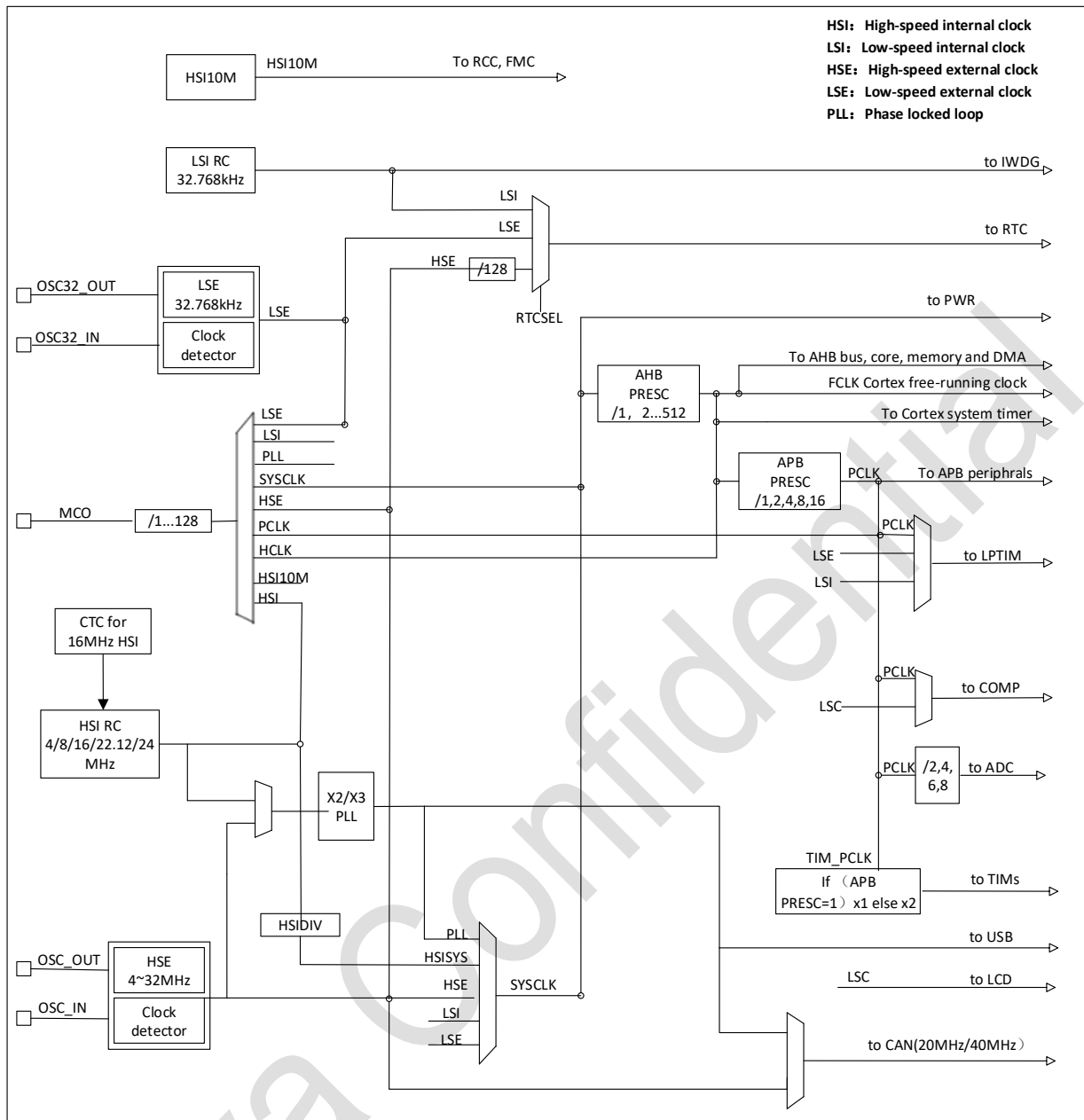


Figure 2-1 System Clock Structure Diagram

## 2.5. Power management

### 2.5.1. Power block diagram

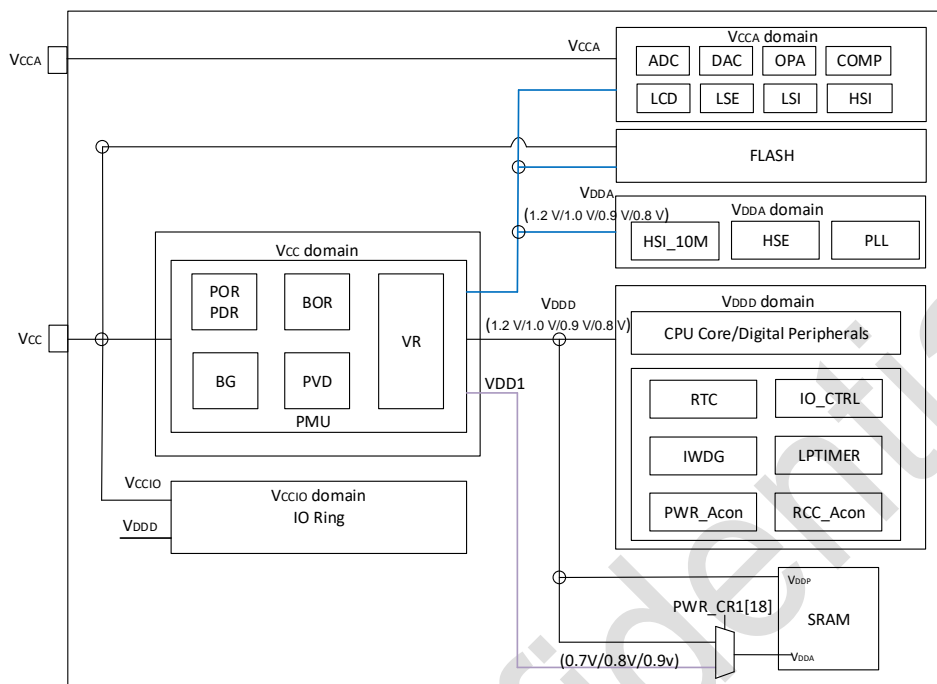


Figure 2-2 Power block diagram

Table 2-2 Power Block Diagram

No.	Power supply	Power value	Describe
1	V <sub>CC</sub>	1.7 to 5.5 V	The chip is supplied power through the power pins.
2	V <sub>DDx</sub> (V <sub>DDD</sub> /V <sub>DDA</sub> )	1.2 V/1.0 V/0.9 V/0.8 V ±10%	VR supplies power to the main logic circuits and SRAM inside the chip. When the MR is powered, it outputs 1.2 V. According to the software configuration, when entering the stop mode it powered by MR or LPR, and the LPR output is determined to be 1.2 V/1.0 V/0.9 V/0.8 V.
3	V <sub>CCA</sub>	1.7 to 5.5 V	The chip is supplied analog power through the power pins.

### 2.5.2. Power monitoring

#### 2.5.2.1. Power on reset (POR/PDR)

The power-on reset (POR) and power-down reset (PDR) module is designed in the chip to provide power-on and power-off reset for the chip. The module keeps working in all modes.

#### 2.5.2.2. Brown-out reset (BOR)

In addition to POR/ PDR, BOR (brown-out reset) is also implemented. BOR can only be enabled and disabled through the option byte .

When the BOR is turned on, the BOR threshold can be selected by the Option byte, and both the rising and falling detection points can be configured individually.

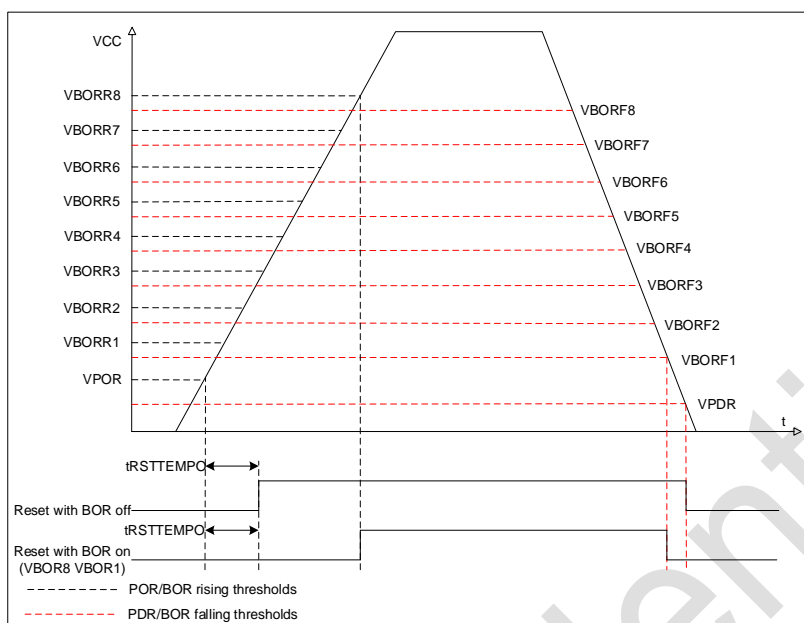


Figure 2-3 POR/PDR/BOR threshold

### 2.5.2.3. Programmable voltage detection (PVD)

Programmable voltage detector (PVD) module can be used to detect the  $V_{CC}$  power supply and the voltage of the PB7 pin, and the detection point is configured through the register. When  $V_{CC}$  is higher or lower than the detection point of PVD, the corresponding reset flag is generated.

This event is internally connected to line 16 of EXTI, depending on the rising/falling edge configuration of EXTI line 16, when  $V_{CC}$  rises above the detection point of PVD, or  $V_{CC}$  falls below the detection point of PVD, an interrupt is generated. In the service program, users can perform urgent shutdown tasks.

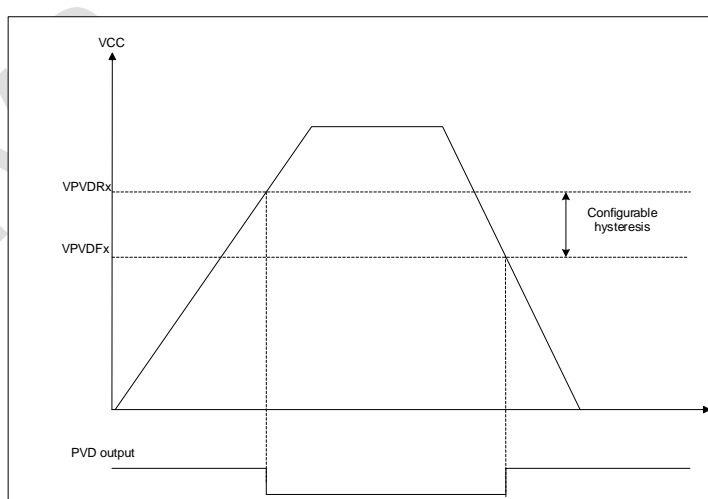


Figure 2-4 PVD threshold

### 2.5.3. Voltage regulator

The regulator has two operating modes:

- Main regulator (MR) is used in normal operating mode.
- Low power regulator (LPR) can be used in Stop mode where the power demand is reduced.

#### 2.5.4. Low-power mode

In addition to the normal operating mode, the chip has 2 low-power modes:

- Sleep mode: Peripherals can be configured to keep working when the CPU clock is off (NVIC, SysTick, etc.). It is recommended only to enable the modules that must work, and close the module after the module works.
- Stop mode: In this mode, the contents of SRAM and registers are maintained, HSI and HSE are turned off, and most modules of clocks in the VDD domain are stopped. GPIO, PVD, COMP output, RTC and LPTIM can wake up stop mode.

### 2.6. Reset

Two resets are designed in the chip: power reset and system reset.

#### 2.6.1. Power reset

A power reset occurs in the following situations:

- Power-on/power-down reset (POR/PDR)
- Brown-out Reset (BOR )

#### 2.6.2. System reset

A system reset occurs when the following events occur:

- Reset of NRST pin
- Windowed watchdog reset (WWDG)
- Independent watchdog reset (IWDG)
- SYSRESETREQ software reset
- Option byte load reset (OBL)
- Power reset (POR/PDR, BOR)

### 2.7. General-purpose inputs and outputs (GPIOs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function, locking mechanism will freeze I/Os configuration function .

### 2.8. Hardware divider (DIV)

Hardware divider is a 32-bit signed/unsigned integer hardware divider.

DIV feature:

- Configurable signed/unsigned integer division calculation
- 32-bit dividend, 32-bit divisor

- Output 32-bit quotient and 32-bit remainder
- Division zero warning flag, division end flag
- 8 clock cycles to complete a division operation
- Write the divisor register to trigger the division operation to start
- Automatically wait for the end of the calculation when reading the quotient register/remainder register

## 2.9. Direct memory access controller (DMA)

Direct memory access (DMA) is used to provide high-speed data transfer between peripherals and memory or between memory and memory. Data can be moved quickly through DMA without CPU intervention, which saves CPU resources for other operations. The DMA controller has seven channels, each dedicated to managing requests for memory access from one or more peripherals. There is also a mediator to coordinate the priority of individual DMA requests.

The main functions are as follows:

- Single AHB Master
- Support peripherals to memory, the memory to the peripherals, memory to memory and peripherals to peripheral data transmission
- On-chip memory devices, such as Flash, an SRAM, AHB and APB peripherals, as the source and target
- All DMA channel can be independent configuration:
  - Each channel is associated either with a DMA request signal from a peripheral or with a software trigger in a memory-to-memory transfer. This configuration is done by software.
  - The priority between requests is programmable by software (4 levels per channel: very high, high, medium, low) and, in equal cases, by hardware (such as a request for channel 1 taking precedence over a request for channel 2).
  - The transfer sizes of the source and destination are independent (byte, half word, word), simulating packing and unpacking. The source and destination addresses must be aligned by data size.
  - Programmable data transmission: 0 ~ 65535
- Each channel generates an interrupt request. Each interrupt request is caused by one of three DMA events: transfer completion, half-transfer, or transfer error.

## 2.10. Interrupts and events

The PY32F072 handles exceptions through the Cortex-M0+ processor's embedded a nested vectored interrupt controller (NVIC) and an extended interrupt/event controller (EXTI).

### 2.10.1. Nested vectored interrupt controller (NVIC)

NVIC is a tightly coupled IP inside the Cortex-M0+ processor. The NVIC can handle NMI (Non-Maskable Interrupts) and maskable external interrupts from outside the processor and Cortex-M0+ internal exceptions. NVIC provides flexible priority management.

The tight coupling of the processor core to the NVIC greatly reduces the delay between an interrupt event and the initiation of the corresponding interrupt service routine (ISR). The ISR vectors are listed in a vector table, stored at a base address of the NVIC. The vector table base address determines the vector address of the ISR to execute, and the ISR is used as the offset composed of serial numbers.

If a high-priority interrupt event occurs and a low-priority interrupt event is just waiting to be serviced, the later-arriving high-priority interrupt event will be serviced first. Another optimization is called tail-chaining. When returning from a high-priority ISR and then starting a pending low-priority ISR, unnecessary pushes and pops of processor contexts will be skipped. This reduces latency and improves power efficiency.

NVIC features:

- Low latency interrupt handling
- Level 4 interrupt priority
- Supports one NMI interrupt
- Support 32 maskable external interrupts
- Supports 10 Cortex-M0+ exceptions
- High-priority interrupts can interrupt low-priority interrupt responses
- Support tail-chaining optimization
- Hardware interrupt vector retrieval

### 2.10.2. Extended interrupt/event controller (EXTI)

EXTI adds flexibility to handle physical wire events and generates wake-up events when the processor wakes up from stop mode.

The EXTI controller has multiple channels, including a maximum of 16 GPIOs, 1 PVD output, 3 COMP outputs, RTC and LPTIM wake-up signals. GPIO, PVD and COMP can be configured to be triggered by a rising edge, falling edge or double edge. Any GPIO signal can be configured as EXTI0 to 15 channel through the select signal.

- Each EXTI line can be independently masked through registers.
- The EXTI controller can capture pulses shorter than the internal clock period.
- Registers in the EXTI controller latch each event. Even in stop mode, after the processor wakes up from stop mode, it can identify the wake-up source or identify the GPIO and event that caused the interrupt.



## 2.11. Analog-to-digital converter (ADC)

The chip has a 12-bit SAR-ADC. The module supports up to 24 conversion channels, including 16 external channels and 8 internal channels. The reference voltage can be selected with precision voltage (2.14 V、2.66 V) or the power supply voltage.

The internal channels are:  $T_{S\_VIN}$ ,  $V_{REFINT}$ ,  $V_{CCA}/3$ , OPA 1~3, DAC 1~2.

- The conversion mode of each channel can be set to single, continuous, sweep, discontinuous mode. Conversion results are stored in left or right-aligned 16-bit data registers.
- An analogue watchdog allows the application to detect if the input voltage exceeds a user-defined high or low threshold.
- The ADC has been implemented to operate at a low frequency, resulting in lower power consumption.
- At the end of sampling, conversion, and continuous conversion, an interrupt request is generated when the conversion voltage exceeds the threshold when simulating the watchdog.

## 2.12. Digital-to-analog converter (DAC)

Digital/analog conversion module (DAC) is a 12-bit digital input, voltage output digital/analog converter. The DAC can be configured in 8-bit or 12-bit mode, or can be used in conjunction with a DMA controller. When the DAC is operating in 12-bit mode, the data can be left justified or right justified. The DAC module has two output channels, each with a separate converter. In dual-DAC mode, the two channels can be converted independently, or they can be converted simultaneously and update the output of the two channels synchronously. The main features are as follows:

- 12 mode data left or right aligned
- synchronous update functionality
- waveform generating noise
- triangle waveform generation
- dual DAC channel or respectively at the same time
- each channel has the DMA function
- support DMA underflow error detection
- external triggers the transformation

## 2.13. Comparators (COMP)

Three general purpose comparators are integrated in the chip, namely COMP1/2/3. It can be used as a separate module or in combination with timer.

Comparators can be used as follows:

- Triggered by analog signal to generate low-power mode wake-up function
- Analog signal conditioning
- Cycle by cycle current control loop when connected with PWM output from timer

## 2.14. Operational amplifier (OPA)

The OPA1/2/3 module can be flexibly configured and is suitable for simple amplifiers. The three internal opamps can be cascaded using external resistors.

OPA features are summarized as follows:

- Three independently configured operational amps
- OPA input range is 0 to  $V_{CCA}$ , output range is 0.1 V to  $V_{CCA} - 0.2$  V (demand) to simulate a module, a programmable gain
- Can be configured for the following models
- General operational mode (general purpose OPA)
- DAC voltage follower

## 2.15. Hardware divider (DIV)

Hardware divider is a 32-bit signed/unsigned integer hardware divider.

DIV features:

- Support 32-bit division
- The data in the register cannot be changed while the current division is not finished
- Configurable signed/unsigned integer division calculation
- 32-bit divisor, 32-bit divisor
- Outputs 32-bit quotient and 32-bit remainder
- Divide-by-zero warning flag bit, end-of-division flag bit
- 8 clock cycles to complete a division operation
- Write the divisor register to trigger the start of the divide operation
- After writing the divisor, when reading the quotient and remainder registers, you need to wait for the completion flag DIV\_END
- When the divisor is 0, the result of quotient and remainder is 0

## 2.16. Liquid crystal display (LCD) controller

The LCD controller is a digital controller/driver for monochrome passive liquid crystal displays (LCDS), with up to 8 common terminals (COM) and 40 segment terminals (SEG) to drive 160 (4 \* 40) or 288 (8 \* 36) LCD image elements. The exact number of terminals depends on the device pins described in the data manual. LCD functions are summarized as follows:

- Highly flexible frame rate control
- Support static, 1/2, 1/3, 1/4, 1/6, and 1/8 of a duty ratio
- Support 1/2, 1/3 bias voltage
- Up to 16 registers LCD data RAM
- By software configuration of LCD contrast

- 3 kinds of waveform generation
  - internal resistance pressure resistance, external pressure, external capacitance partial pressure
  - by way of internal resistance of the software configuration partial pressure power consumption, so as to match the capacitance charge needed for the LCD panel
- Support low power consumption modes: LCD controller can be on the Run, Sleep and Stop mode for display
- Configurable frame interrupt
- Support LCD flashing function and configuration of multiple flicker frequency
- Unused LCD segments and public pin can be configured to digital or analog functions

## 2.17. Timer

The characteristics of different timers of PY32F072 series are shown in the following table:

Table 2-3 Timer features comparison

Timer type	Timer	Counter resolution	Counter type	Prescaler factor	DMA	Capture /compare channels	Complementary outputs
Advanced control	TIM1	16-bit	Up, down, center aligned	Integer from 1 to 65536	Support	4	3
General purpose	TIM2	32-bit	Up, down, center aligned	Integer from 1 to 65536	Support	4	-
General purpose	TIM3	16-bit	Up, down, center aligned	Integer from 1 to 65536	Support	4	-
	TIM14	16-bit	Up	Integer from 1 to 65536	-	1	-
	TIM15	16-bit	Up	Integer from 1 to 65536	-	2	1
	TIM16, TIM17	16-bit	Up	Integer from 1 to 65536	Support	1	1
Basic	TIM6, TIM7	16-bit	Up	Integer from 1 to 65536	Support	-	-

### 2.17.1. Advanced-control timer (TIM1)

The advanced-control timer (TIM1) is consist of a 16-bit auto-reload counter driven by a programmable prescaler. It can be used in various scenarios, including pulse length measurement of input signals (input capture) or generating output waveforms (output compare, output PWM, complementary PWM with dead-time insertion).

TIM1 includes 4 independent channels:

- Input capture
- Output comparison
- PWM generation (edge or center-aligned mode)
- Single pulse mode output

If TIM1 is configured as a standard 16-bit timer, it has the same features as the TIMx timer. If configured as the 16-bit PWM generator, it has full modulation capability (0-100%).

The counter can can be frozen in debug mode.

Many features are shared with those of the standard timers which have the same architecture. The advanced control timer can therefore work together with the other timers by the Timer Link feature for synchronization or event chaining.

TIM1 supports the DMA function.

## 2.17.2. General-purpose timers

### 2.17.2.1. TIM2/TIM3

The general-purpose timers TIM2/TIM3 are consist of 32/16-bit auto-reload counters and a 32/16-bit prescaler. There are four independent channels each for input capture/output compare, PWM or one-pulse mode output.

- They can work with the TIM1 by the Timer Link.
- TIM2/TIM3 supports DMA function.
- This timer is capable of handling quadrature (incremental) encoder signals and the digital outputs from 1 to 3 hall-effect sensors.
- The counter can be frozen in debug mode.

### 2.17.2.2. TIM14

- The general-purpose timer (TIM14) is consist of a 16-bit auto-reload counter driven by a programmable prescaler.
- TIM14 features one single channel for input capture/output compare, PWM or one-pulse mode output.
- The counter can be frozen in debug mode.

### 2.17.2.3. TIM15/TIM16/TIM17

- The general-purpose timer (TIM15, TIM16 and TIM17) is consist of a 16-bit auto-reload counter driven by a programmable prescaler.
- TIM16/TIM17 features one single channel for input capture/output compare, PWM or one-pulse mode output.
- TIM15 features two single channel for input capture/output compare, PWM or one-pulse mode output.
- TIM15/TIM16/TIM17 have complementary outputs with dead time.
- TIM15/TIM16/TIM17 supports DMA function.
- The counter can be frozen in debug mode.

### 2.17.3. Basic timers (TIM6/TIM7)

- The basic timer (TIM6/TIM7) is consist of a 16-bit auto-reload upcounter driven by their programmable prescaler respectively.
- Synchronization circuit to trigger DAC.
- Generate interrupt/DMA request on update event (counter overflow).

### 2.17.4. Low power timer (LPTIM)

- LPTIM is a 16 -bit upcounter with a 3-bit prescaler and only support a single count.
- LPTIM can be configured as a stop mode wake-up source.
- The counter can be frozen in debug mode.

### 2.17.5. Independent watchdog (IWDG)

Independent watchdog (IWDG) is integrated in the chip, and this module has the characteristics of high-security level, accurate timing and flexible use. IWDG finds and resolves functional confusion due to software failure and triggers a system reset when the counter reaches the specified timeout value.

- The IWDG is clocked by LSI, so even if the main clock fails, it can keep working.
- IWDG is the best suited for applications that require the watchdog as a standalone process outside of the main application and do not have high timing accuracy constraints.
- Controlling of option byte can enable IWDG hardware mode.
- IWDG is the wake-up source of stop mode, which wakes up stop mode by reset.
- The counter can be frozen in debug mode.

### 2.17.6. System window watchdog (WWDG)

The system window watchdog is based on a 7-bit downcounter that can be set as free running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the APB clock (PCLK). It has an early warning interrupt capability, and the counter can be frozen in debug mode.

### 2.17.7. SysTick timer

SysTick timer is dedicated to real-time operating systems, but could also be used as a standard downcounter.

SysTick Features:

- 24-bit down counter
- Auto-reload capability
- Maskable system interrupt generation when the counter reaches 0

## 2.18. Real-time clock (RTC)

The real-time clock is an independent counter. It has a set of continuous counting counters, which can provide a clock calendar function under the corresponding software configuration. Modifying the value of the counter can reset the current time and date of the system.

- RTC is a 32-bit programmable counter with a prescale factor of up to  $2^{20}$  bits.
- The RTC counter clock source can be LSE/LSI and the stop wake-up source.
- RTC can generate alarm interrupt, second interrupt and overflow interrupt (maskable).
- RTC supports clock calibration.
- RTC can be frozen in debug mode.

## 2.19. Cyclic redundancy check cell(CRC)

CRC computing unit is based on a fixed generation polynomial to obtain 32-bit CRC computing results. In other applications, CRC technology is mainly used to verify the correctness and integrity of data transmission or data storage. CRC cell contains one 32-bit data register:

- When writing to this register, as an input register, you can enter new data to perform CRC calculations.
- When the register is read, the result of the last CRC calculation is returned.
- Each time a data register is written, the result of the calculation is a combination of the previous CRC calculation and the new calculation (CRC calculation is performed on the entire 32-bit word rather than byte by byte).
- You can RESET register CRC\_DR to 0xFFFF by setting the reset bit of register CRC\_CR. This operation does not affect the data in register CRC\_IDR.
- The initial CRC value can be configured.

## 2.20. Clock check system (CTC)

The clock calibration controller (CTC) uses hardware to automatically calibrate the RC crystal oscillator (HSI) when the internal configuration is 16 MHz, and uses the PLL (48 M) after 3 times the frequency as the clock source of the USB module. The CTC module calibrates the HSI clock frequency based on an external high-precision reference signal source, and adjusts the calibration value automatically or manually to obtain an accurate PLL48 M clock.

The CTC module performs the following functions:

- Three external reference sources: GPIO, LSE clock, USB\_D\_SOF.
- Provide software reference synchronization pulse.
- Hardware calibration automatically, no software operation.
- 16 bits calibration counter with reference source capture and overload capabilities.
- 8 bits clock calibration base value for frequency evaluation and automatic calibration.

- Flag bits and interrupts that indicate the state of clock calibration: calibration success state (CKOKIF), Warning state (CKWARNIF), and error state (ERRIF).

## 2.21. System configuration controller (SYSCFG)

The SYSCFG module provides the following functions:

- The filtering function on the IO pin of the  $I^2C$  type was enabled or disabled
- Enable or disable filtering on all I/O pins
- Remap trigger sources for some Dmas to different DMA channels
- Remap memory at the beginning of the code interval (Boot)
- Manages the TIMERS ETR or brake input

## 2.22. Debug support (DBG)

The MCU DBG module assists the debugger with the following functions:

- Support sleep mode, stop mode and standby mode
- When the CPU enters the HALT mode, the control timer or watchdog stops counting or continues counting
- Block  $I^2C1$  and  $I^2C2$  SMBUS timeouts when the CPU is in HALT mode
- Block CAN's receive register from updating allocation tracking pins when the CPU enters HALT
- The MCUIDBG register also provides chip ID encoding. This ID encoding can be accessed by a JTAG or SW debug interface, or by a user program.

## 2.23. Inter-integrated circuit interface ( $I^2C$ )

$I^2C$  (inter-integrated circuit) bus interface connects the microcontroller and the serial  $I^2C$  bus. It provides multi-master capability and controls all  $I^2C$  bus specific sequences, protocols, arbitration and timing. Standard mode (Sm) and fast mode (Fm) are supported.

$I^2C$  Features:

- Two  $I^2C$  Interface, support Slave and Master mode
- Multi-host function : can be Master or Slave
- Support different communication speeds
  - Standard Mode (Sm): Up to 100 kHz
  - Fast Mode (Fm): up to 400 kHz
- As Master
  - Generate Clock
  - Generation of Start and Stop
- As Slave
  - Programmable  $I^2C$  address detection
  - Dual-address capability that responds to two secondary addresses
  - Discovery of the Stop bit

- 7-bit/10-bit addressing mode
- General call
- Status flag
  - Transmit/receive mode flags
  - Byte transfer complete flag
  - I<sup>2</sup>C busy flag bit
- Error flag
  - Master arbitration loss
  - ACK failure after address/data transfer
  - Start/Stop error
  - Overrun/Underrun (clock stretching function disable)
- Optional clock stretching
- Single-byte buffer with DMA capability
- Software reset
- Analog noise filter function
- Support SMBus

## 2.24. Universal synchronous/asynchronous receiver transmitter (USART)

PY32F072 contains 4 USARTs, supports ISO7816, LIN, IrDA.

The USARTs provide a flexible method for full-duplex data exchange with external devices using the industry-standard NRZ asynchronous serial data format. The USART utilizes a fractional baudrate generator to provide a wide range of baudrate options.

It supports simultaneous one-way communication and half-duplex single-wire communication, and it also allows multi-processor communication.

Automatic baudrate detection is supported.

High-speed data communication can be achieved by using the DMA method of the multi-buffer configuration.

USARTs features:

- Full-duplex asynchronous communication
- NRZ standard format
- Configurable 16 times or 8 times oversampling for increased flexibility in speed and clock tolerance
- Programmable baudrate shared by transmit and receive, up to 4.5 Mbit/s
- Automatic baudrate detection
- Programmable data length of 8 or 9 bits
- Configurable stop bits (0.5, 1, 1 or 2 bits)
- Synchronous mode and clock output function for synchronous communication
- Single-wire half-duplex communication



- Independent transmit and receive enable bits
- Hardware flow control
- Receive/transmit bytes by DMA buffer
- Detection flag
  - Receive full buffer
  - Send empty buffer
  - End of transmission
- Parity control
  - Send check digit
  - Check the received data
- Flagged interrupt sources
  - CTS change
  - Send empty register
  - Send completed
  - Receive full data register
  - Bus idle detected
  - Overflow error
  - Frame error
  - Noise operation
  - Error detection
- Multiprocessor communication
  - If the address does not match, enter silent mode
- Wake-up from silent mode: by idle detection and address flag detection

## 2.25. Serial peripheral interface (SPI)

PY32F072 contains two SPIs. SPIs allow the chip to communicate with external devices in half-duplex, full-duplex, and simplex synchronous serial communication. This interface can be configured in Master mode and provides the communication clock (SCK) for external slave devices. The interface can also work in a multi-master configuration.

The SPI features are as follows:

- Master or Slave mode
- 3-wire full-duplex simultaneous transmission
- 2-wire half-duplex synchronous transmission (with bidirectional data line)
- 2-wire simplex synchronous transmission (no bidirectional data line)
- 8-bit or 16-bit transmission frame selection
- Support multi-master mode
- 8 Master mode baud rate prescale factors (max  $f_{PCLK}/2$ )
- Slave mode frequency (max  $f_{PCLK}/4$ )
- Both Master and Slave modes can be managed by software or hardware NSS: dynamic change of Master/Slave operating mode

- Programmable clock polarity and phase
- Programmable data order, MSB first or LSB first
- Dedicated transmit and receive flags that can trigger interrupts
- SPI bus busy status flag
- Motorola mode
- Interrupt-causing Master mode faults, overloads
- Two 32-bit Rx and Tx FIFOs with DMA capability

## 2.26. USB2.0 full-speed module

PY32F072 contains 1 USB 2.0 full speed module. USB peripheral implements the interface between USB2.0 full speed bus and APB1 bus. Support USB suspend/restore operation, can stop the device clock to achieve low power consumption. The main features are as follows:

- Comply with the technical specifications of USB 2.0 full speed devices
- It can be configured with 1 to 6 USB endpoints
- CRC(cyclic redundancy check) generation/check, reverse non-return to zero (NRZI) encoding/decoding and bit filling
- Support control transmission/synchronous transmission/batch transmission/interrupt transmission
- Supports a dual buffer mechanism for batch/synchronous endpoints
- USB suspend and restore operations are supported
- Frame lock clock pulse generation
- Dedicated 1024-byte packet cache storage

## 2.27. CAN

PY32F072 contains one CAN communication interface module. The Controller Area Network (CAN) bus is a bus standard that can realize the communication between microprocessors or devices without a host.

The CAN bus controller CAN handle data sending and receiving on the bus. In this product, the CAN controller has 12 groups of filters. Filters are used to select messages for the application to receive. The application program in the CAN controller can Transmit 1 Primary Transmit Buffer (PTB) and 3 Secondary Transmit buffers (PTB) STB) sends the sending data to the bus, and the sending scheduler determines the sending order of the mailboxes. The bus data is obtained through three Receive buffers (RB). Three STBS and three RB can be interpreted as two level 3 FIFO, where the FIFO is completely hardware controlled. The CAN bus controller also supports Time-trigger communication.

- Fully support ISO11898-1 CAN2.0A/ CAN2.0B protocol
- CAN2.0 supports a maximum communication baud rate of 1M bit/s
- The baud rate ranges from 1 to 1/256. The baud rate is flexibly configured
- Three receive buffers
  - FIFO mode

- Error or unreceived data does not overwrite stored messages
- One high - priority primary send buffer PTB
- Three sub-send buffers STB
  - FIFO mode
  - Priority arbitration mode
- 12 separate sets of filters
  - It supports 11-bit standard ID and 29-bit extended ID
  - Programmable ID CODE bit and MASK bit
- Silent mode support
- Supports loopback mode
- Supports capturing transmission error types and locating quorum failure locations
- Programmable error warning value
- Support ISO11898-4 time trigger CAN and receive time stamp

## 2.28. Serial wire debug (SWD)

The ARM SWD interface allows serial debugging tools to be connected to the PY32F072.

### 3. Pin Configuration

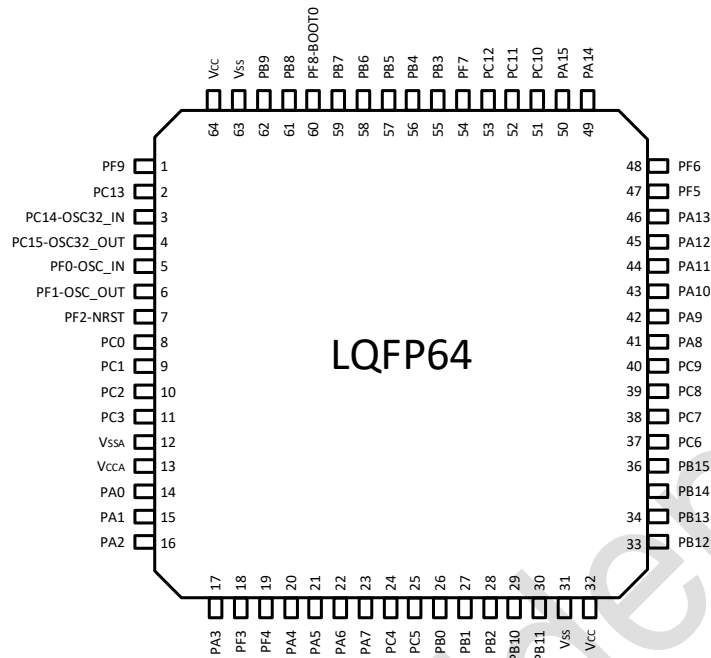


Figure 3-1 LQFP64 PY32F072R1xT6 Pinout1 (Top view)

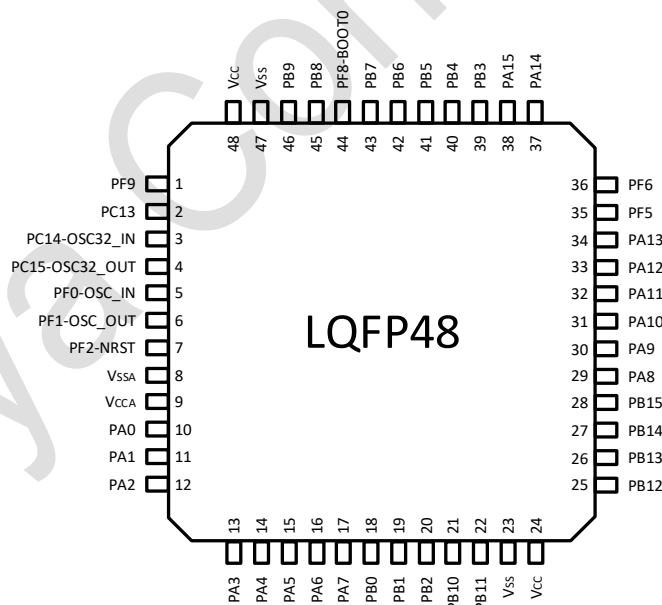


Figure 3-2 LQFP48 PY32F072C1xTx Pinout1 (Top view)

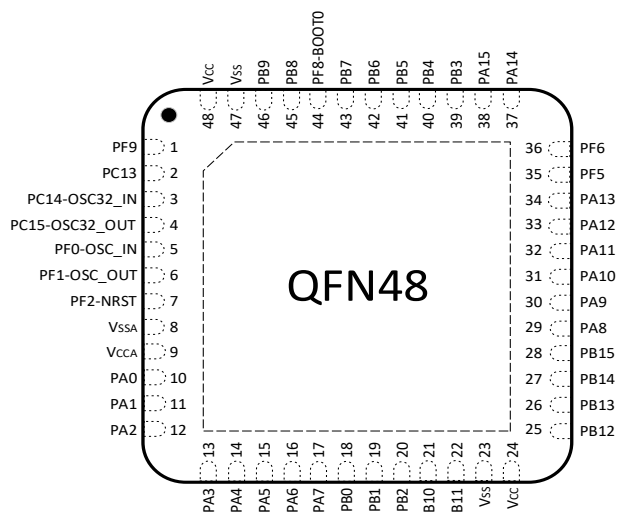


Figure 3-3 QFN48 PY32F072C1xU6 Pinout1 (Top view)

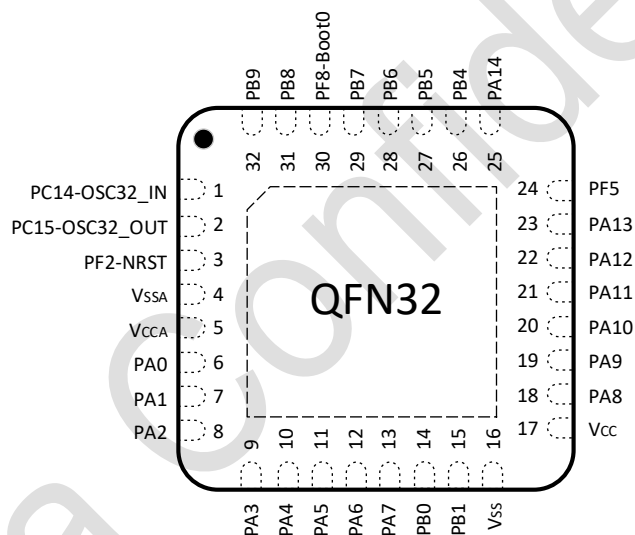


Figure 3-4 QFN32(5\*5) PY32F072K1xU6 Pinout1 / QFN32(4\*4) PY32F072K3xU7 Pinout3 (Top view)

Table 3-1 Pin Definition Terminology and Symbols

Name	Symbol	Definition
Pin type	S	Supply pin
	G	Ground pin
	I	Input-only pin
	I/O	Input/output pin
I/O structure	COM	Normal 5V I/O with analog input and output function
	RST	Reset pin, with internal weak pull-up resistor, without analog input and output function
	COM_F	I/O, I <sup>2</sup> C Fm+ capable with analog input and output function
	COM_U	GPIO 5V tolerant with USB PHY function

Name		Symbol	Definition
Notes		-	Unless otherwise specified, all ports are used as floating inputs between and after reset
Pin function	Alternate functions	-	Function selected by GPIOx_AFR register
	Additional functions	-	Directly selected or enabled through peripheral registers

Table 3-2 pin definition

package				Reset	Ports Type	Ports structure	Port Functions	
LQFP64 R1	LQFP48 C1	QFN48 C1	QFN32 K1 / K3				Alternate functions	Additional functions
1	1	1	-	PF9	I/O	COM	-	-
2	2	2	-	PC13	I/O	COM	SPI1_SCK/I <sup>2</sup> S1_CK TIM1_BKIN	-
3	3	3	1	PC14	I/O	COM	TIM1_BKIN2	OSC32_IN
4	4	4	2	PC15	I/O	COM	TIM15_BKIN	OSC32_OUT
5	5	5	-	PF0-OSC_IN	I/O	COM	CTC_SYNC USART2_TX TIM1_BKIN TIM14_CH1	OSC_IN
6	6	6	-	PF1-OSC_OUT	I/O	COM	USART2_RX TIM1_CH1N TIM15_CH1N	OSC_OUT
7	7	7	3	PF2-NRST <sup>(1)</sup>	I/O	RST	TIM1_CH2 EVENTOUT MCO	-
8	-	-	-	PC0	I/O	COM	EVENTOUT SPI1_MISO/I <sup>2</sup> S1_MC USART2_CTS USART3_RTS	ADC_IN10, COMP1_INP0, COMP2_INN0, SEG27
9	-	-	-	PC1	I/O	COM	EVENTOUT SPI1_MOSI/I <sup>2</sup> S1_SD USART2_RTS USART3_CTS TIM15_CH1	ADC_IN11, COMP1_INP1, COMP2_INN1, SEG26
10	-	-	-	PC2	I/O	COM	EVENTOUT SPI2_MISO/I <sup>2</sup> S2_MC USART3_TX USART3_RX TIM15_CH2	ADC_IN12, COMP1_INP2, COMP2_INN2, SEG25

package				Reset	Ports Type	Ports structure	Port Functions	
LQFP64 R1	LQFP48 C1	QFN48 C1	QFN32 K1 / K3				Alternate functions	Additional functions
11	-	-	-	PC3	I/O	COM	EVENTOUT SPI2_MOSI/I <sup>2</sup> S2_SD USART3_RX USART3_TX	ADC_IN13, COMP1_INP3, COMP2_INN3, SEG24
12	8	8	4	V <sub>SSA</sub>	G		Ground	
13	9	9	5	V <sub>CCA</sub>	S		Analog power supply	
14	10	10	6	PA0	I/O	COM	USART2_CTS TIM2_CH1_ETR USART4_TX COMP1_OUT SPI2_SCK	ADC_IN0, COMP1_INP4, COMP1_INN0, COMP2_INP0, COMP2_INN4, SEG23
15	11	11	7	PA1	I/O	COM	EVENTOUT USART2_RTS TIM2_CH2 USART4_RX TIM15_CH1N I <sup>2</sup> C1_SMBA SPI1_SCK/I <sup>2</sup> S1_CK SPI2_MOSI	ADC_IN1, COMP1_INP5, COMP1_INN1, COMP2_INP1, COMP2_INN5, SEG22
16	12	12	8	PA2	I/O	COM	TIM15_CH1 USART2_TX TIM2_CH3 COMP2_OUT SPI1_MOSI/I <sup>2</sup> S1_SD SPI2_MISO	ADC_IN2, COMP1_INP6, COMP1_INN2, COMP2_INP2, SEG21
17	13	13	9	PA3	I/O	COM	EVENTOUT TIM15_CH2 USART2_RX TIM2_CH4 SPI2_MISO SPI2_NSS/I <sup>2</sup> S2_WS	ADC_IN3, COMP1_INP7, COMP1_INN3, COMP2_INP3, SEG20
18	-	-	-	PF3	I/O	COM_F	EVENTOUT I <sup>2</sup> C1_SCL I <sup>2</sup> C2_SCL	-
19	-	-	-	PF4	I/O	COM_F	I <sup>2</sup> C1_SDA I <sup>2</sup> C2_SDA	-
20	14	14	10	PA4	I/O	COM	EVENTOUT SPI1_NSS/I <sup>2</sup> S1_WS	ADC_IN4, DAC_OUT1,

package				Reset	Ports Type	Ports structure	Port Functions	
LQFP64 R1	LQFP48 C1	QFN48 C1	QFN32 K1 / K3				Alternate functions	Additional functions
							USART2_CK TIM14_CH1 SPI2_MOSI USART2_TX PVD_OUT	COMP1_INP8, COMP1_INN4, COMP2_INP4, SEG19
21	15	15	11	PA5	I/O	COM	EVENTOUT SPI1_SCK/I <sup>2</sup> S1_CK TIM2_CH1_ETR USART3_TX	ADC_IN5, DAC_OUT2, COMP1_INP9, COMP1_INN5, COMP2_INP5, COMP3_INP0, COMP3_INN0, SEG18, OPA2_OUT
22	16	16	12	PA6	I/O	COM	EVENTOUT SPI1_MISO/I <sup>2</sup> S1_MC TIM3_CH1 TIM1_BKIN USART3_CTS TIM16_CH1 COMP1_OUT	ADC_IN6, COMP1_INP10COMP 1_INN6, OPA2_INN, SEG17
23	17	17	13	PA7	I/O	COM	EVENTOUT SPI1_MOSI/I <sup>2</sup> S1_SD TIM3_CH2 TIM1_CH1N TIM14_CH1 TIM17_CH1 COMP2_OUT	ADC_IN7, COMP1_INP11COMP 1_INN7, OPA2_INP, SEG16
24	-	-	-	PC4	I/O	COM	EVENTOUT USART3_TX COMP3_OUT SPI1_NSS/I <sup>2</sup> S1_WS USART1_TX TIM2_CH1_ETR IR_OUT	ADC_IN14, COMP1_INN8, SEG15
25	-	-	-	PC5	I/O	COM	USART3_RX SPI1_MOSI/I <sup>2</sup> S1_SD USART1_RX TIM2_CH2	ADC_IN15, COMP1_INN9, SEG14
26	18	18	14	PB0	I/O	COM	EVENTOUT TIM3_CH3	ADC_IN8, COMP2_INN6,



package				Reset	Ports Type	Ports structure	Port Functions	
LQFP64 R1	LQFP48 C1	QFN48 C1	QFN32 K1 / K3				Alternate functions	Additional functions
							TIM1_CH2N USART3_CK COMP1_OUT SPI1_NSS/I <sup>2</sup> S1_WS USART3_RX	SEG13
27	19	19	15	PB1	I/O	COM	EVENTOUT TIM14_CH1 TIM3_CH4 TIM1_CH3N USART3_RTS COMP3_OUT	ADC_IN9, COMP2_INP6, COMP2_INN7, COMP3_INP1, COMP3_INN1, SEG12
28	20	20	-	PB2	I/O	COM	EVENTOUT SPI2_MISO USART3_TX	COMP2_INP7, COMP2_INN8, SEG11
29	21	21	-	PB10	I/O	COM_F	I <sup>2</sup> C2_SCL TIM2_CH3 USART3_TX SPI2_SCK/I <sup>2</sup> S2_CK COMP1_OUT USART2_RTS I <sup>2</sup> C1_SCL	COMP2_INP8, SEG10
30	22	22	-	PB11	I/O	COM_F	EVENTOUT I <sup>2</sup> C2_SDA TIM2_CH4 USART3_RX COMP2_OUT SPI2_MOSI USART2_CTS I <sup>2</sup> C1_SDA	COMP3_INP8, COMP3_INN4, SEG9
31	23	23	16	V <sub>SS</sub>	G		Ground	
32	24	24	17	V <sub>CC</sub>	S		Digital power supply	
33	25	25	-	PB12	I/O	COM	EVENTOUT SPI2_NSS/I <sup>2</sup> S2_WS TIM1_BKIN USART3_CK TIM15_BKIN	COMP2_INP9, OPA3_INN, SEG8
34	26	26	-	PB13	I/O	COM_F	EVENTOUT SPI2_SCK/I <sup>2</sup> S2_CK TIM1_CH1N	COMP2_INP10, OPA3_INP, SEG7

package				Reset	Ports Type	Ports structure	Port Functions	
LQFP64 R1	LQFP48 C1	QFN48 C1	QFN32 K1 / K3				Alternate functions	Additional functions
							USART3_CTS	
							I <sup>2</sup> C2_SCL	
							MCO	
							TIM15_CH1N	
							I <sup>2</sup> C1_SCL	
35	27	27	-	PB14	I/O	COM_F	EVENTOUT SPI2_MISO/I <sup>2</sup> S2_MC TIM15_CH1 TIM1_CH2N USART3_RTS I <sup>2</sup> C2_SDA I <sup>2</sup> C1_SDA	COMP2_INP11, COMP3_INP9, COMP3_INN5, OPA3_OUT, SEG6
36	28	28	-	PB15	I/O	COM	EVENTOUT SPI2_MOSI/I <sup>2</sup> S2_SD TIM15_CH2 TIM1_CH3N TIM15_CH1N	SEG5
37	-	-	-	PC6	I/O	COM	TIM3_CH1 SPI2_SCK/I <sup>2</sup> S2_CK USART4_RX TIM2_CH3	SEG4
38	-	-	-	PC7	I/O	COM	TIM3_CH2 SPI2_MISO/I <sup>2</sup> S2_MC USART4_TX TIM2_CH4	COMP3_INP13 COMP3_INN8, SEG3
39	-	-	-	PC8	I/O	COM	TIM3_CH3 SPI2_MOSI/I <sup>2</sup> S2_SD USART4_CTS TIM1_CH1	SEG2
40	-	-	-	PC9	I/O	COM	TIM3_CH4 SPI2_NSS/I <sup>2</sup> S2_WS I <sup>2</sup> S1_CKIN USART4_RTS TIM1_CH2	SEG1
41	29	29	18	PA8	I/O	COM	EVENTOUT MCO USART1_CK TIM1_CH1 CTC_SYNC	SEG0, OPA1_OUT

package				Reset	Ports Type	Ports structure	Port Functions	
LQFP64 R1	LQFP48 C1	QFN48 C1	QFN32 K1 / K3				Alternate functions	Additional functions
							SPI2_NSS	
							USART1_TX	
42	30	30	19	PA9	I/O	COM_F	EVENTOUT	COM0, OPA1_INP
							TIM15_BKIN	
							USART1_TX	
							TIM1_CH2	
							I <sup>2</sup> C1_SCL	
							SPI2_MISO	
							MCO	
							I <sup>2</sup> C2_SCL	
43	31	31	20	PA10	I/O	COM_F	EVENTOUT	COM1, OPA1_INN
							TIM17_BKIN	
							USART1_RX	
							TIM1_CH3	
							I <sup>2</sup> C1_SDA	
							SPI2_MOSI	
							I <sup>2</sup> C2_SDA	
44	32	32	21	PA11	I/O	COM_U	EVENTOUT	USB_DM, COM2, CAN_RX
							USART1_CTS	
							TIM1_CH4	
							COMP1_OUT	
							SPI1_MISO/I <sup>2</sup> S1_MC	
45	33	33	22	PA12	I/O	COM_U	EVENTOUT	USB_DP, COM3, CAN_TX
							USART1_RTS	
							TIM1_ETR	
							COMP2_OUT	
							SPI1_MOSI/I <sup>2</sup> S1_SD	
							I <sup>2</sup> S1_CKIN	
46	34	34	23	PA13 <sup>(2)</sup>	I/O	COM	EVENTOUT	-
							SWDIO	
							IR_OUT	
							USART1_RX	
							COMP3_OUT	
							PVD_OUT	
47	35	35	24	PF5	I/O	COM	TIM1_BKIN2	RTC_OUT
48	36	36	-	PF6	I/O	COM	USART1_CTS	-
49	37	37	25	PA14 <sup>(2)</sup>	I/O	COM	EVENTOUT	-
							SWCLK	

package				Reset	Ports Type	Ports structure	Port Functions	
LQFP64 R1	LQFP48 C1	QFN48 C1	QFN32 K1 / K3				Alternate functions	Additional functions
							USART2_TX	
							USART1_TX	
							PVD_OUT	
50	38	38	-	PA15	I/O	COM	EVENTOUT	
							SPI1_NSS/I <sup>2</sup> S1_WS	
							USART2_RX	
							TIM2_CH1_ETR	
							USART4_RTS	
							USART3_RTS_DE_C	
51	-	-	-	PC10	I/O	COM	USART4_TX	COM4/SEG39
							USART3_TX	
							TIM1_CH3	
52	-	-	-	PC11	I/O	COM	USART4_RX	COM5/SEG38
							USART3_RX	
							TIM1_CH4	
53	-	-	-	PC12	I/O	COM	USART4_CK	COM6/SEG37
							USART3_CK	
							TIM14_CH1	
54	-	-	-	PF7	I/O	COM	TIM3_ETR	COM7/SEG36
							USART3_RTS	
							TIM1_CH1N	
55	39	39	-	PB3	I/O	COM	EVENTOUT	COMP2_INN9, SEG35/VLCDH
							SPI1_SCK/I <sup>2</sup> S1_CK	
							TIM2_CH2	
							USART1_RTS_DE_C	
							TIM1_CH2	
56	40	40	26	PB4	I/O	COM	EVENTOUT	COMP1_INP12 COMP2_INP12SEG34 /VLCD3
							SPI1_MISO/I <sup>2</sup> S1_MC	
							TIM3_CH1	
							USART1_CTS	
							USART1_CK	
							TIM1_CH2N	
							TIM17_BKIN	
57	41	41	27	PB5	I/O	COM	SPI1_MOSI/I <sup>2</sup> S1_SD	COMP1_INP13SEG33 /VLCD2
							TIM3_CH2	
							TIM16_BKIN	
							I <sup>2</sup> C1_SMBA	
							USART1_CK	
							COMP2_OUT	

package				Reset	Ports Type	Ports structure	Port Functions	
LQFP64 R1	LQFP48 C1	QFN48 C1	QFN32 K1 / K3				Alternate functions	Additional functions
							USART1_RTS	
							USART1_TX	
							TIM1_CH3N	
58	42	42	28	PB6	I/O	COM_F	EVENTOUT	COMP1_INP14COMP 2_INP14SEG32/VLCD 1
							USART1_TX	
							I <sup>2</sup> C1_SCL	
							TIM16_CH1N	
							SPI2_MISO	
							USART3_CTS	
							TIM1_CH3	
							I <sup>2</sup> C2_SCL	
							EVENTOUT	
USART1_RX								
I <sup>2</sup> C1_SDA								
TIM17_CH1N								
USART4_CTS								
SPI2_MOSI								
I <sup>2</sup> C2_SDA								
TIM1_CH1								
60	44	44	30	PF8/BOOT <sup>(3)</sup>	I/O	COM	SEG30	
61	45	45	31	PB8	I/O	COM_F	EVENTOUT	SEG29, CAN_RX
							I <sup>2</sup> C1_SCL	
							I <sup>2</sup> C2_SCL	
							TIM16_CH1	
							SPI2_SCK	
							USART1_TX	
							USART3_TX	
							TIM15_BKIN	
TIM1_CH1N								
62	46	46	32	PB9	I/O	COM_F	EVENTOUT	SEG28, CAN_TX
							IR_OUT	
							I <sup>2</sup> C1_SDA	
							TIM17_CH1	
							SPI2_NSS/I <sup>2</sup> S2_WS	
							USART1_RX	
							USART3_RX	
I <sup>2</sup> C2_SDA								
63	47	47	-	V <sub>SS</sub>	G	-	Ground	
64	48	48	-	V <sub>CC</sub>	S	-	Digital power supply	

1. Configure by option bytes to choose PF2 or NRST.
2. After reset, PA13 and PA14 are configured as SWDIO and SWCLK AF functions, the former has an internal pull-up resistor and the latter has an internal pull-down resistor activated.
3. BOOT0 defaults to digital input mode and pull-down is enable.

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### 3.1. PortA alternate function mapping

Table 3-3 PortA alternate function mapping

PortA	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PA0	-	USART2_CTS	TIM2_CH1_ETR	-	USART4_TX	-	-	COMP1_OUT	SPI2_SCK	-	-	-	-	-	-	-
PA1	EVENTOUT	USART2_RTS	TIM2_CH2	-	USART4_RX	TIM15_CH1N	I <sup>2</sup> C1_SMBA	-	SPI1_SCK/ I <sup>2</sup> S1_CK	SPI2_MOSI	-	-	-	-	-	-
PA2	TIM15_CH1	USART2_TX	TIM2_CH3	-	-	-	-	COM2_OUT	SPI1_MOSI/ I <sup>2</sup> S1_SD	SPI2_MISO	-	-	-	-	-	-
PA3	TIM15_CH2	USART2_RX	TIM2_CH4	-	-	-	-	EVENTOUT	SPI2_MSIO	SPI2_NSS/ I <sup>2</sup> S2_WS	-	-	-	-	-	-
PA4	SPI1_NSS/ I <sup>2</sup> S1_WS	USART2_CK	-	-	TIM14_CH1	-	-	EVENTOUT	SPI2_MOSI	USART2_TX	-	-	PVD_OUT	-	-	-
PA5	SPI1_SCK/ I <sup>2</sup> S1_CK	-	TIM2_CH1_ETR	-	-	-	-	EVENTOUT	-	-	USART3_TX	-	-	-	-	-
PA6	SPI1_MISO/ I <sup>2</sup> S1_MCK	TIM3_CH1	TIM1_BKIN	-	USART3_CTS	TIM16_CH1	EVENTOUT	COMP1_OUT	-	-	-	-	-	-	-	-
PA7	SPI1_MOSI/ I <sup>2</sup> S1_SD	TIM3_CH2	TIM1_CH1N	-	TIM14_CH1	TIM17_CH1	EVENTOUT	COMP2_OUT	-	-	-	-	-	-	-	-
PA8	MCO	USART1_CK	TIM1_CH1	EVENTOUT	CTC_SYNC	-	-	-	SPI2_NSS	-	USART1_TX	-	-	-	-	-
PA9	TIM15_BKIN	USART1_TX	TIM1_CH2	-	-	-	I <sup>2</sup> C1_SCL	EVENTOUT	SPI2_MISO	MCO	-	-	-	I <sup>2</sup> C2_SCL	-	-
PA10	TIM17_BKIN	USART1_RX	TIM1_CH3	-	-	-	I <sup>2</sup> C1_SDA	EVENTOUT	SPI2_MOSI	-	-	-	-	I <sup>2</sup> C2SDA	-	-
PA11	EVENTOUT	USART1_CTS	TIM1_CH4	-	CAN_RX	-	-	COMP1_OUT	SPI1_MISO/ I <sup>2</sup> S1_MCK	-	-	TIM1_BKIN2	-	-	-	-
PA12	EVENTOUT	USART1_RTS	TIM1_ETR	-	CAN_TX	-	-	COMP2_OUT	SPI1_MOSI/ I <sup>2</sup> S1_SD	I <sup>2</sup> S1_CKIN	-	-	-	-	-	-
PA13	SWDIO	IROUT	-	-	-	-	-	EVENTOUT	-	USART1_RX	-	COMP3_OUT	PVD_OUT	-	-	-
PA14	SWCLK	USART2_TX	-	-	-	-	-	EVENTOUT	-	USART1_TX	-	-	PVD_OUT	-	-	-
PA15	SPI1_NSS/ I <sup>2</sup> S1_WS	USART2_RX	TIM2_CH1_ETR	EVENTOUT	USART4_RTS	-	-	EVENTOUT	-	-	USART3_RT S_DE_CK	-	-	-	-	-

### 3.2. PortB alternate function mapping

Table 3-4 Port B alternate function mapping

PortB	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PB0	EVENTOUT	TIM3_CH3	TIM1_CH2N	-	USART3_CK	-	-	COMP1_OUT	SPI1_NSS/ I <sup>2</sup> S1_WS	-	USART3_RX	-	-	-	-	-
PB1	TIM14_CH1	TIM3_CH4	TIM1_CH3N	-	USART3_RTS	-	-	EVENTOUT	-	-	-	COMP3_OUT	-	-	-	-
PB2	-	-	-	-	-	-	-	EVENTOUT	SPI2_MIS O	-	USART3_TX	-	-	-	-	-
PB3	SPI1_SCK/ I <sup>2</sup> S1_CK	EVENT- TOUT	TIM2_CH2	-	USART1_RTS	-	-	EVENTOUT	-	-	-	TIM1_CH2	-	-	-	-
PB4	SPI1_MISO/ I <sup>2</sup> S1_MCK	TIM3_CH1	EVENTOUT	-	USART1_CTS	TIM17_BKIN	-	-	-	-	-	TIM1_CH2N	-	USART1_CK	-	-
PB5	SPI1_MOSI/ I <sup>2</sup> S1_SD	Tim3_CH2	TIM16_BKIN	I <sup>2</sup> C1_SMBA	USART1_CK	-	-	COM2_OUT	-	USART1_RTS	-	TIM1_CH3N	-	USART1_TX	-	-
PB6	USART1_TX	I <sup>2</sup> C1_SCL	TIM16_CH1N	-	-	-	-	EVENTOUT	SPI2_MIS O	-	USART3_CTS	TIM1_CH3	-	I <sup>2</sup> C2_SCL	-	-
PB7	USART1_RX	I <sup>2</sup> C1_SDA	TIM17_CH1N	-	USART4_CTS	-	-	EVENTOUT	SPI2_MOS I	-	-	TIM1_CH1	-	I <sup>2</sup> C2_SDA	-	-
PB8	-	I <sup>2</sup> C1_SCL	TIM16_CH1	-	CAN_RX	-	-	EVENTOUT	SPI2_SCK	USART1_TX	USART3_TX	TIM15_BKIN	-	I <sup>2</sup> C2_SCL	TIM1_CH1N	-
PB9	IR_OUT	I <sup>2</sup> C1_SDA	TIM17_CH1	EVENTOUT	CAN_TX	SPI2_NSS/ I <sup>2</sup> S2_WS	-	-	-	USART1_RX	USART3_RX	-	-	I <sup>2</sup> C2_SDA	-	-
PB10	-	I <sup>2</sup> C2_SCL	TIM2_CH3	-	USART3_TX	SPI2_SCK/ I <sup>2</sup> S2_CK	-	COMP1_OUT	-	USART2_RTS	-	-	-	I <sup>2</sup> C1_SCL	-	-
PB11	EVENTOUT	I <sup>2</sup> C2_SDA	TIM2_CH4	-	USART3_RX	-	-	COMP2_OUT	SPI2_MOS I	USART2_CTS	-	-	-	I <sup>2</sup> C1_SDA	-	-
PB12	SPI2_NSS/ I <sup>2</sup> S2_WS	EVENT- TOUT	TIM1_BKIN	-	USART3_CK	TIM15_BKIN	-	-	-	-	-	-	-	-	-	-
PB13	SPI2_SCK/ I <sup>2</sup> S2_CK	-	TIM1_CH1N	-	USART3_CTS	I <sup>2</sup> C2_SCL	-	EVENTOUT	-	MCO	-	TIM15_CH1N	-	I <sup>2</sup> C1_SCL	-	-
PB14	SPI2_MISO/ I <sup>2</sup> S2_MCK	TIM15_CH 1	TIM1_CH2N	-	USART3_RTS	I <sup>2</sup> C2_SDA	-	EVENTOUT	-	-	-	TIM15_CH1	-	I <sup>2</sup> C1_SDA	-	-
PB15	SPI2_MOSI/ I <sup>2</sup> S2_SD	TIM15_CH 2	TIM1_CH3N	TIM15_CH1N	-	-	-	EVENTOUT	-	-	-	-	-	-	-	-



### 3.3. PortC alternate function mapping

Table 3-5 PortC alternate function mapping

PortC	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PC0	EVENTOUT	-	-	-	-	-	-	-	SPI1_MISO/I <sup>2</sup> S1_MCK	USART2_CTS	USART3_RTS	-	-	-	-	-
PC1	EVENTOUT	-	-	-	-	-	-	-	SPI1_MOSI/I <sup>2</sup> S1_SD	USART2_RTS	USART3_CTS	TIM15_CH1	-	-	-	-
PC2	EVENTOUT	SPI2_MISO/I <sup>2</sup> S2_MCK	-	-	-	-	-	-	-	USART3_TX	USART3_RX	TIM15_CH2	-	-	-	-
PC3	EVENTOUT	SPI2_MOSI/I <sup>2</sup> S2_SD	-	-	-	-	-	-	-	USART3_RX	USART3_TX	-	-	-	-	-
PC4	EVENTOUT	USART3_TX	-	-	-	-	-	COMP3_OUT	SPI1_NSS/I <sup>2</sup> S1_WS	USART1_TX	-	TIM2_CH1_ETR	IR_OUT	-	-	-
PC5	-	USART3_RX	-	-	-	-	-	-	SPI1_MOSI/I <sup>2</sup> S1_SD	USART1_RX	-	TM2_CH2	-	-	-	-
PC6	TIM3_CH1	-	-	-	-	-	-	-	SPI2_SCK/I <sup>2</sup> S2_CK	-	USART4_RXD	TIM2_CH3	-	-	-	-
PC7	TIM3_CH2	-	-	-	-	-	-	-	SPI2_MISO/I <sup>2</sup> S2_MCK	-	USART4_TX	TIM2_CH4	-	-	-	-
PC8	TIM3_CH3	-	-	-	-	-	-	-	SPI2_MOSI/I <sup>2</sup> S2_SD	-	USART4_CTS	TIM1_CH1	-	-	-	-
PC9	TIM3_CH4	-	-	-	-	-	-	-	SPI2_NSS/I <sup>2</sup> S2_WS	I <sup>2</sup> S1_CKIN	USART4_RTS	TIM1_CH2	-	-	-	-
PC10	USART4_TX	USART3_TX	-	-	-	-	-	-	-	-	-	TIM1_CH3	-	-	-	-
PC11	USART4_RX	USART3_RX	-	-	-	-	-	-	-	-	-	TIM1_CH4	-	-	-	-
PC12	USART4_CK	USART3_CK	-	-	-	-	-	-	-	-	-	TIM14_CH1	-	-	-	-
PC13	-	-	-	-	-	-	-	-	SPI1_SCK/I <sup>2</sup> S1_CK	-	-	TIM1_BKIN	-	-	-	-
PC14	-	-	-	-	-	-	-	-	-	-	-	TIM1_BKIN2	-	-	-	-
PC15	-	-	-	-	-	-	-	-	-	-	-	TIM15_BKIN	-	-	-	-

### 3.4. PortF alternate function mapping

Table 3-7 PortF alternate function mapping

PortC	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PC0	EVENTOUT	-	-	-	-	-	-	-	SPI1_MISO/I <sup>2</sup> S1_MCK	USART2_CTS	USART3_RTS	-	-	-	-	-
PC1	EVENTOUT	-	-	-	-	-	-	-	SPI1_MOSI/I <sup>2</sup> S1_SD	USART2_RTS	USART3_CTS	TIM15_CH1	-	-	-	-
PC2	EVENTOUT	SPI2_MISO/I <sup>2</sup> S2_MCK	-	-	-	-	-	-	-	USART3_TX	USART3_RX	TIM15_CH2	-	-	-	-
PC3	EVENTOUT	SPI2_MOSI/I <sup>2</sup> S2_SD	-	-	-	-	-	-	-	USART3_RX	USART3_TX	-	-	-	-	-

PortC	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PC4	EVENTOUT	USART3_TX	-	-	-	-	-	COMP3_OUT	SPI1_NSS/I2S1_WS	USART1_TX	-	TIM2_CH1_ETR	IR_OUT	-	-	-
PC5	-	USART3_RX	-	-	-	-	-	-	SPI1_MOSI/I2S1_SD	USART1_RX	-	TIM2_CH2	-	-	-	-
PC6	TIM3_CH1	-	-	-	-	-	-	-	SPI2_SCK/I2S2_CK	-	USART4_RXD	TIM2_CH3	-	-	-	-
PC7	TIM3_CH2	-	-	-	-	-	-	-	SPI2_MISO/I2S2_MCK	-	USART4_TX	TIM2_CH4	-	-	-	-
PC8	TIM3_CH3	-	-	-	-	-	-	-	SPI2_MOSI/I2S2_SD	-	USART4_CTS	TIM1_CH1	-	-	-	-
PC9	TIM3_CH4	-	-	-	-	-	-	-	SPI2_NSS/I2S2_WS	I2S1_CKIN	USART4_RTS	TIM1_CH2	-	-	-	-
PC10	USART4_TX	USART3_TX	-	-	-	-	-	-	-	-	-	TIM1_CH3	-	-	-	-
PC11	USART4_RX	USART3_RX	-	-	-	-	-	-	-	-	-	TIM1_CH4	-	-	-	-
PC12	USART4_CK	USART3_CK	-	-	-	-	-	-	-	-	-	TIM14_CH1	-	-	-	-
PC13	-	-	-	-	-	-	-	-	SPI1_SCK/I2S1_CK	-	-	TIM1_BKIN	-	-	-	-
PC14	-	-	-	-	-	-	-	-	-	-	-	TIM1_BKIN2	-	-	-	-
PC15	-	-	-	-	-	-	-	-	-	-	-	TIM15_BKIN	-	-	-	-

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# 4. Memory Map

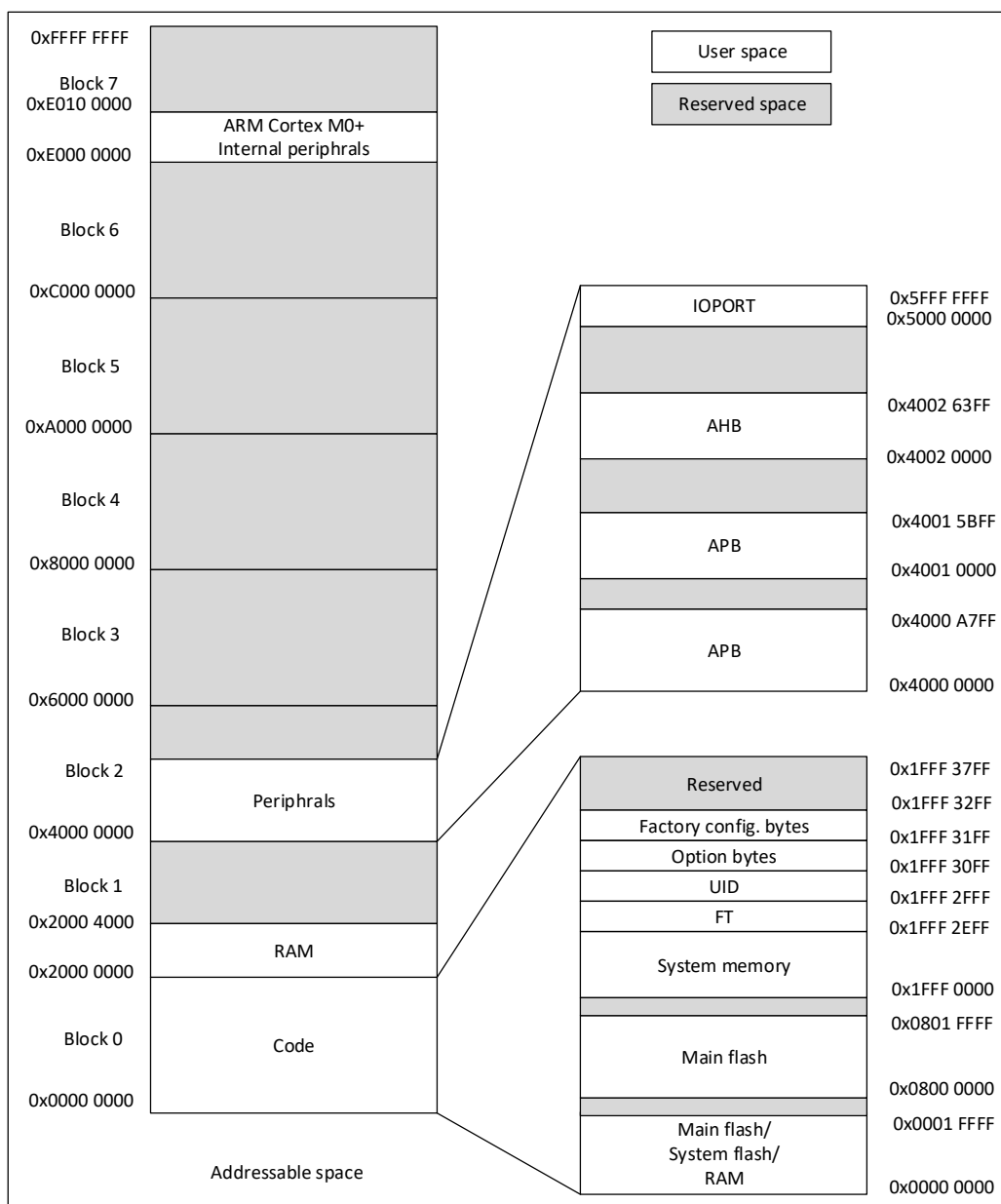


Figure 4-1 Memory map

Table 4-1 Memory boundary address

Type	Boundary Address	Size	Memory Area	Description
SRAM	0x2000 4000-0x3FFF FFFF	-	Reserved	
	0x2000 0000-0x2000 3FFF	16 KB	SRAM	SRAM 最大为 16 KB
Code	0x1FFF 3400-0x1FFF FFFF	-	Reserved	-
	0x1FFF 3300-0x1FFF 33FF	256 Bytes	FT infor1 bytes	Flash Verify Value, Analog 和 Flash Trimming, Debug ID.
	0x1FFF 3200-0x1FFF 32FF	256 Bytes	FT infor0 bytes	Normal TS DATA, High TS DATA, HSI Re-Trim data,

Type	Boundary Address	Size	Memory Area	Description
				Flash/SRAM size configuration.
	0x1FFF 3100-0x1FFF 31FF	256 Bytes	Option bytes	option bytes information, IP enable <sup>(1)</sup>
	0x1FFF 3000-0x1FFF 30FF	256 Bytes	UID bytes	Unique ID
	0x1FFF 0000-0x1FFF 2FFF	12 KB	System memory	Boot loader
	0x0802 0000-0x1FFE FFFF	-	Reserved	-
	0x0800 0000-0x0801 FFFF	128 KB	Main flash memory	-
	0x0002 0000-0x07FF FFFF	-	Reserved	-
	0x0000 0000-0x0001 FFFF	128 KB	Selected based on Boot configuration, 1) Main flash memory 2) System memory 3) SRAM	

1. The address is marked as Reserved , which cannot be written , read as 0 , and a response error is generated .

Table 4-2 Peripheral register boundary address<sup>(1)</sup>

Bus	Boundary Address	Size	Peripheral
	0xE000 000-0xE00F FFFF	1MB	M0+
IOPORT	0x5000 1800 - 0x5FFF FFFF	-	Reserved
	0x5000 1400 - 0x5000 17FF	1 KB	GPIOF
	0x5000 1000 - 0x5000 13FF	1 KB	Reserved
	0x5000 0C00 - 0x5000 0FFF	1 KB	Reserved
	0x5000 0800 - 0x5000 0BFF	1 KB	GPIOC
	0x5000 0400 - 0x5000 07FF	1 KB	GPIOB
	0x5000 0000 - 0x5000 03FF	1 KB	GPIOA
AHB	0x4002 4000 - 0x4FFF FFFF	-	Reserved
	0x4002 3C00 - 0x4002 3FFF	-	Reserved
	0x4002 3800 - 0x4002 3BFF	1 KB	DIV
	0x4002 3400 - 0x4002 37FF	1 KB	Reserved
	0x4002 3000 - 0x4002 33FF	1 KB	CRC
	0x4002 2400 - 0x4002 2FFF	-	Reserved
	0x4002 2000 - 0x4002 23FF	1 KB	Flash
	0x4002 1C00 - 0x4002 1FFF	-	Reserved
	0x4002 1800 - 0x4002 1BFF	1 KB	EXTI
	0x4002 1400 - 0x4002 17FF	-	Reserved
	0x4002 1000 - 0x4002 13FF	1 KB	RCC <sup>(2)</sup>
	0x4002 0400 - 0x4002 0FFF	-	Reserved
	0x4002 0000 - 0x4002 03FF	1 KB	DMA
APB	0x4001 5C00 - 0x4001 FFFF	-	Reserved
	0x4001 5800 - 0x4001 5BFF	1 KB	DBG

Bus	Boundary Address	Size	Peripheral
	0x4001 4C00 - 0x4001 57FF	-	Reserved
	0x4001 4800 - 0x4001 4BFF	1 KB	TIM17
	0x4001 4400 - 0x4001 47FF	1 KB	TIM16
	0x4001 4000 - 0x4001 43FF	1 KB	TIM15
	0x4001 3C00 - 0x4001 3FFF	-	Reserved
	0x4001 3800 - 0x4001 3BFF	1 KB	USART1
	0x4001 3400 - 0x4001 37FF	-	Reserved
	0x4001 3000 - 0x4001 33FF	1 KB	SPI1/I2S1
	0x4001 2C00 - 0x4001 2FFF	1 KB	TIM1
	0x4001 2800 - 0x4001 2BFF	-	Reserved
	0x4001 2400 - 0x4001 27FF	1 KB	ADC
	0x4001 0400 - 0x4001 23FF	-	Reserved
	0x4001 0300 - 0x4001 03FF	1 KB	OPA
	0x4001 0200 - 0x4001 02FF		COMP
	0x4001 0000 - 0x4001 01FF		SYSCFG
	0x4000 8000 - 0x4000 FFFF	-	Reserved
	0x4000 7C00 - 0x4000 7FFF	1 KB	LPTIM1
	0x4000 7800 - 0x4000 7BFF	-	Reserved
	0x4000 7400 - 0x4000 77FF	1 KB	DAC
	0x4000 7000 - 0x4000 73FF	1 KB	PWR <sup>(3)</sup>
	0x4000 6C00 - 0x4000 6FFF	1 KB	CTC
	0x4000 6800 - 0x4000 6BFF	-	Reserved
	0x4000 6400 - 0x4000 67FF	1 KB	CAN
	0x4000 6000 - 0x4000 63FF	1 KB	USB SRAM
	0x4000 5C00 - 0x4000 5FFF	1 KB	USB
	0x4000 5800 - 0x4000 5BFF	1 KB	I <sup>2</sup> C2
	0x4000 5400 - 0x4000 57FF	1 KB	I <sup>2</sup> C1
	0x4000 5000 - 0x4000 53FF	-	Reserved
	0x4000 4C00 - 0x4000 4FFF	1 KB	USART4
	0x4000 4800 - 0x4000 4BFF	1 KB	USART3
	0x4000 4400 - 0x4000 47FF	1 KB	USART2
	0x4000 3C00 - 0x4000 43FF	-	Reserved
	0x4000 3800 - 0x4000 3BFF	1 KB	SPI2/I2S2
	0x4000 3400 - 0x4000 37FF	1 KB	Reserved
	0x4000 3000 - 0x4000 33FF	1 KB	IWDG
	0x4000 2C00 - 0x4000 2FFF	1 KB	WWDG
	0x4000 2800 - 0x4000 2BFF	1 KB	RTC
	0x4000 2400 - 0x4000 27FF	1 KB	LCD
	0x4000 2000 - 0x4000 23FF	1 KB	TIM14
	0x4000 1800 - 0x4000 1FFF	-	Reserved

Bus	Boundary Address	Size	Peripheral
	0x4000 1400 - 0x4000 17FF	1 KB	TIM7
	0x4000 1000 - 0x4000 13FF	1 KB	TIM6
	0x4000 0800 - 0x4000 0FFF	-	Reserved
	0x4000 0400 - 0x4000 07FF	1 KB	TIM3
	0x4000 0000 - 0x4000 03FF	1 KB	TIM2

1. In the above table, the reserved address cannot be written, read back is 0, and a hardfault is generated
2. Not only supports 32 bits word access, but also supports halfword and byte access.
3. Not only supports 32 bits word access, but also supports halfword access.

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## 5. Electrical Characteristics

### 5.1. Parameter conditions

Unless otherwise specified, all voltages are referenced to  $V_{SS}$ .

#### 5.1.1. Minium and maximum values

Unless otherwise specified, the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at  $T_A = 25^\circ\text{C}$  and  $T_A = T_{A(\text{max})}$  (given by the selected temperature range).

Data based on electrical characterization results, design simulations and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation.

#### 5.1.2. Typical values

Unless otherwise specified, typical data is based on  $T_A = 25^\circ\text{C}$  and  $V_{CC} = 3.3\text{V}$ . They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than equal to the value indicated.

### 5.2. Absolute maximum ratings

Stresses above the absolute maximum ratings listed in following tables may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 5-1 Voltage characteristics <sup>(1)</sup>

Symbol	Ratings	Minimum	Maximum	Unit
$V_{CC}$	External mains power supply	-0.3	6.25	V
$V_{IN}$	Input voltage of other pins	-0.3	$V_{CC}+0.3$	V

- Power supply  $V_{CC}$  and ground  $V_{SS}$  pins must always be connected to the external power supply within the allowable range.

Table 5-2 Current characteristics

Symbol <sup>(2)</sup>	Describe	Maximum	Unit
$I_{VCC}$	Flowing into $V_{CC}$ pin (supply current) <sup>(1)</sup>	150	mA
$I_{VSS}$	Total current flowing out of $V_{SS}$ pin (outflow current) <sup>(1)</sup>	150	
$I_{IO(\text{PIN})}$	Output current sunk by any I/O and control pin	20	
	Output current source by any I/Os and control pin	-20	

1. Power supply  $V_{CC}$  and ground  $V_{SS}$  pins must always be connected to the external power supply within the allowable range.
2. These I/O types refer to the terms and symbols defined by pins.

Table 5-3 Thermal characteristics

Symbol	Describe	Condition	Value	Unit
$T_{STG}$	Storage temperature range		-65 to +150	°C
$T_O$	Range of operating temperature	x 6 version	-40 to +85	°C
		x 7 version	-40 to +105	

### 5.3. Operating conditions

#### 5.3.1. General operating conditions

Table 5-4 General operating conditions

Symbol	Parameter	Condition	Minimum	Maximum	Unit
$f_{HCLK}$	Internal AHB clock frequency	-	0	72	MHz
$f_{PCLK}$	Internal APB Clock frequency	-	0	72	MHz
$V_{CC}$	Standard operating voltage	-	1.7	5.5	V
$V_{CCA}$	Operating voltage of analog circuit	Must be the same as $V_{CC}$	1.7	5.5	V
$V_{IN}$	I/O input voltage	-	-0.3	$V_{CC}+0.3$	V
$T_A$	Ambient temperature	-	-40	85	°C
		-	-40	105	
$T_J$	Junction temperature	-	-40	90	°C
		-	-40	110	

#### 5.3.2. Operating conditions at power-up / power-down

Table 5-5 Operating conditions at power-up / power-down

Symbol	Parameter	Condition	Minimum	Maximum	Unit
$t_{VCC}$	$V_{CC}$ rise time rate	-	0	$\infty$	us/V
	$V_{CC}$ fall time rate	-	20	$\infty$	

#### 5.3.3. Embedded reset and PVD module features

Table 5-6 Embedded reset module features

Symbol	Parameter	Condition	Minimum	Typical	Maximum	Unit
$V_{PVD}$	Programmable voltage detector level selection	PLS[2:0]=000 (Rising edge)	1.7	1.8	1.9	V
		PLS[2:0]=000 (Falling edge)	1.6	1.7	1.8	V
		PLS[2:0]=001 (Rising edge)	1.9	2	2.1	V
		PLS[2:0]=001 (Falling edge)	1.8	1.9	2	V
		PLS[2:0]=010 (Rising edge)	2.1	2.2	2.3	V
		PLS[2:0]=010 (Falling edge)	2	2.1	2.2	V
		PLS[2:0]=011 (Rising edge)	2.3	2.4	2.5	V



Symbol	Parameter	Condition	Minimum	Typical	Maximum	Unit
		PLS[2:0]=011 (Falling edge)	2.2	2.3	2.4	V
		PLS[2:0]=100 (Rising edge)	2.5	2.6	2.7	V
		PLS[2:0]=100 (Falling edge)	2.4	2.5	2.6	V
		PLS[2:0]=101 (Rising edge)	2.7	2.8	2.9	V
		PLS[2:0]=101 (Falling edge)	2.6	2.7	2.8	V
		PLS[2:0]=110 (Rising edge)	2.9	3	3.1	V
		PLS[2:0]=110 (Falling edge)	2.8	2.9	3	V
		PLS[2:0]=111 (Rising edge)	3.1	3.2	3.3	V
		PLS[2:0]=111 (Falling edge)	3	3.1	3.2	V
V <sub>PVDhyst</sub> <sup>(1)</sup>	PVD hysteresis	-	-	100	-	mV
V <sub>POR/PDR</sub>	Power-on/power-off reset threshold	Rising edge	1.5	1.6	1.7	V
		Falling edge	1.45	1.55	1.65	V
V <sub>PDRhyst</sub> <sup>(1)</sup>	PDR hysteresis	-	-	20	-	mV
V <sub>BOR</sub>	BOR Indicates the threshold voltage	BOR_LEV[2:0]=000 (Rising edge)	1.7	1.8	1.9	V
		BOR_LEV[2:0]=000 (Falling edge)	1.6	1.7	1.8	V
		BOR_LEV[2:0]=001 (Rising edge)	1.9	2	2.1	V
		BOR_LEV[2:0]=001 (Falling edge)	1.8	1.9	2	V
		BOR_LEV[2:0]=010 (Rising edge)	2.1	2.2	2.3	V
		BOR_LEV[2:0]=010 (Falling edge)	2	2.1	2.2	V
		BOR_LEV[2:0]=011 (Rising edge)	2.3	2.4	2.5	V
		BOR_LEV[2:0]=011 (Falling edge)	2.2	2.3	2.4	V
		BOR_LEV[2:0]=100 (Rising edge)	2.5	2.6	2.7	V
		BOR_LEV[2:0]=100 (Falling edge)	2.4	2.5	2.6	V
		BOR_LEV[2:0]=101 (Rising edge)	2.7	2.8	2.9	V
		BOR_LEV[2:0]=101 (Falling edge)	2.6	2.7	2.8	V
		BOR_LEV[2:0]=110 (Rising edge)	2.9	3	3.1	V
		BOR_LEV[2:0]=110 (Falling edge)	2.8	2.9	3	V
		BOR_LEV[2:0]=111 (Rising edge)	3.1	3.2	3.3	V
BOR_LEV[2:0]=111 (Falling edge)	3	3.1	3.2	V		
V <sub>BOR_hyst</sub>	BOR hysteresis voltage	-	-	100	-	mV

1. Guaranteed by design, not tested in production.

### 5.3.4. Operating current characteristics

Table 5-7 Current consumption in run mode

Symbol	Condition						Typical <sup>(1)</sup>	Maximum <sup>(1)</sup>		Unit
	System clock	Frequency	Code	Run	Peripheral clock	Flash sleep		T <sub>A</sub> =85 °C	T <sub>A</sub> =105 °C	
I <sub>DD</sub> (run)	PLL*3 PLL*2	72 MHz	While <sup>(1)</sup>	Flash	ON	DISABLE	8.37	12.7	-	mA
					OFF	DISABLE	4.60	7.80	-	
		48 MHz			ON	DISABLE	6.54	9.73	-	
					OFF	DISABLE	4.01	6.46	-	
	HSI	24 MHz			ON	DISABLE	3.82	6.57	-	
					OFF	DISABLE	2.60	5.07	-	
		16 MHz			ON	DISABLE	2.78	4.94	-	
					OFF	DISABLE	1.90	2.75	-	
8 MHz	ON	DISABLE	1.80	3.40	-					

Symbol	Condition						Typical (1)	Maximum (1)		Unit	
	System clock	Frequency	Code	Run	Peripheral clock	Flash sleep		T <sub>A</sub> = 85 °C	T <sub>A</sub> = 105 °C		
		4 MHz			OFF	DISABLE	1.21	2.73	-	uA	
					ON	DISABLE	1.04	2.22	-		
					OFF	DISABLE	0.87	1.34	-		
	LSI	32.768 kHz				ON	DISABLE	350	825		-
						OFF	DISABLE	293	771		-
						ON	ENABLE	277	721		-
						OFF	ENABLE	225	663		-

1. Data is based on assessment results and is not tested in production.

Table 5-8 Current consumption in sleep mode

Symbol	Condition				Typical (1)	Maximum (1)		Unit	
	System clock	Frequency	Peripheral clock	Flash sleep		T <sub>A</sub> =85 °C	T <sub>A</sub> =105 °C		
I <sub>DD</sub> (sleep)	PLL*3 PLL*2	72 MHz	ON	DISABLE	6.16	8.36	-	mA	
			OFF	DISABLE	2.13	3.14	-		
		48 MHz	ON	DISABLE	4.57	6.34	-		
			OFF	DISABLE	1.82	2.73	-		
	HSI	24 MHz	ON	DISABLE	2.12	3.21	-		
			OFF	DISABLE	0.89	1.54	-		
		16 MHz	ON	DISABLE	1.56	2.75	-		
			OFF	DISABLE	0.71	1.53	-		
		8 MHz	ON	DISABLE	1.01	1.73	-		
			OFF	DISABLE	0.53	1.01	-		
		4 MHz	ON	DISABLE	0.74	1.40	-		
			OFF	DISABLE	0.46	0.91	-		
	LSI	32.768 KHz	ON	DISABLE	349	825	-		uA
			OFF	DISABLE	293	771	-		
		32.768 KHz	ON	ENABLE	278	721	-		
			OFF	ENABLE	224	663	-		

1. Data is based on assessment results and is not tested in production.

Table 5-9 Current consumption in stop mode

Symbol	Condition					Typical (1)	Maximum		Unit
	V <sub>CC</sub>	V <sub>DDx</sub>	MR/LPR	LSI	Peripheral clock		T <sub>A</sub> = 85 °C	T <sub>A</sub> = 105 °C	
I <sub>DD</sub> (stop)	1.7 ~ 5.5 V	1.2 V	MR	-	-	130	245	-	uA
					ON	RTC + IWDG + LPTIM	9.20	135	
		1.2 V	LPR	ON	IWDG	9.30	135	-	
					LPTIM	9.30	135	-	
					RTC	9.20	135	-	
					No	9.00	136	-	
		1.0 V	ON	RTC + IWDG + LPTIM	7.20	106	-		
				IWDG	7.30	106	-		

Symbol	Condition					Typical (1)	Maximum		Unit				
	V <sub>CC</sub>	V <sub>DDx</sub>	MR/LPR	LSI	Peripheral clock		T <sub>A</sub> = 85 °C	T <sub>A</sub> = 105 °C					
				OFF	LPTIM	7.30	106	-					
					RTC	7.20	106	-					
					No	7.00	106	-					
					ON	RTC + IWDG + LPTIM	6.20	93.4		-			
						IWDG	6.30	93.0		-			
						LPTIM	6.30	92.7		-			
				ON	0.9V			OFF		No	6.00	92.8	-
								ON		RTC + IWDG + LPTIM	5.20	84.3	-
										IWDG	5.30	84.1	-
										LPTIM	5.30	83.7	-
										RTC	5.20	84.0	-
								OFF		No	5.00	83.9	-
				ON	0.8 V			OFF		No	5.00	83.9	-

1. Data is based on assessment results and is not tested in production.

### 5.3.5. Wakeup time from low-power modes

Table 5-10 Wakeup time from low-power modes

Symbol	Parameters <sup>(1)</sup>		Condition	Typical <sup>(2)</sup>	Maximum	Unit
t <sub>WUSLEEP</sub>	Wake-up from sleep mode		-	7	-	CPU Cycles
t <sub>WUSTOP</sub>	Wake-up from stop mode	Powered by MR	Execute program in Flash, HSI (24 MHz) as system clock	3.5	-	us
		Powered by LPR	Execute program in Flash, HSI (24 MHz) as system clock	7	-	

1. The wake-up time is measured from the wake-up time until the first instruction is read by the user program.
2. Data is based on assessment results and is not tested in production.

### 5.3.6. External clock source characteristics

#### 5.3.6.1. External high-speed clock

In bypass mode of HSE (the HSEBYP of RCC\_CR is set), when the high-speed start-up circuit in the chip stops working, the corresponding I/O is used as a standard GPIO.

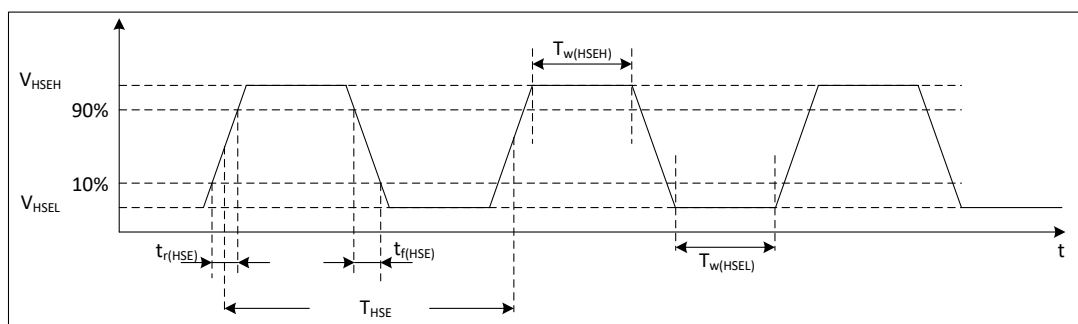


Figure 5-1 External high-speed clock timing diagram

Table 5-11 External high-speed clock features

Symbol	Parameters <sup>(1)</sup>	Minimum	Typical	Maximum	Unit
$f_{HSE\_ext}$	User external clock source frequency	1	8	32	MHz
$V_{HSEH}$	Input pin high level voltage	$0.7V_{CC}$	-	$V_{CC}$	V
$V_{HSEL}$	Input pin low level voltage	$V_{SS}$	-	$0.3V_{CC}$	
$t_w^{(HSEH)}$ $t_w^{(HSEL)}$	Enter high or low time	15	-	-	ns
$t_r^{(HSE)}$ $t_f^{(HSE)}$	Enter the rise/fall time	-	-	20	ns

1. Guaranteed by design, not tested in production.

### 5.3.6.2. External low-speed clock

In the bypass mode of LSE (the LSE BYP of RCC\_BDCR is set), the low-speed start-up circuit in the chip stops working, and the corresponding I/O is used as a standard GPIO.

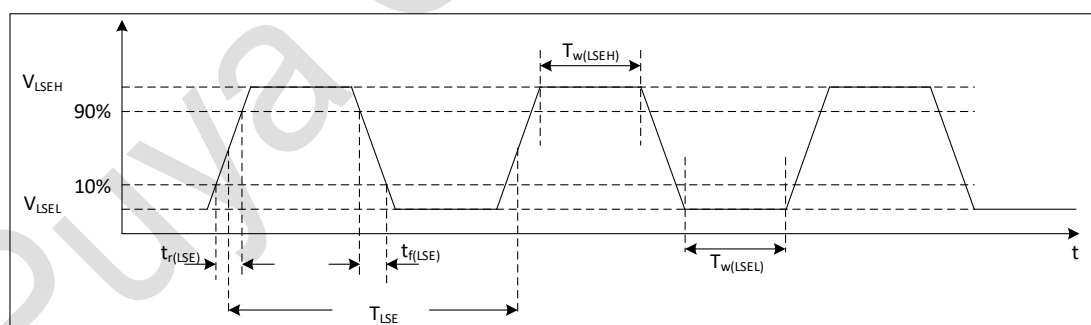


Figure 5-2 External low-speed clock timing diagram

Table 5-12 External low-speed clock characteristics

Symbol	Parameters <sup>(1)</sup>	Minimum	Typical	Maximum	Unit
$f_{LSE\_ext}$	User external clock frequency	-	32.768	1000	kHz
$V_{LSEH}$	Input pin high level voltage	$0.7V_{CC}$	-	-	V
$V_{LSEL}$	Input pin low level voltage	-	-	$0.3V_{CC}$	V
$t_w^{(LSEH)}$ $t_w^{(LSEL)}$	Enter high or low time	450	-	-	ns

$t_{r(LSE)}$	Enter the rise/fall time	-	-	50	ns
$t_{f(LSE)}$					

1. Guaranteed by design, not tested in production .

### 5.3.6.3. External high-speed crystal

The high-speed external (HSE) clock can be supplied with 4 ~ 32 MHz crystal/ceramic resonator oscillator. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time.

Table 5-13 External high-speed crystal characteristics

Symbol	Parameter	Condition <sup>(1)</sup>	Minimum <sup>(2)</sup>	Typical	Maximum <sup>(2)</sup>	Unit
$f_{OSC\_IN}$	Oscillation frequency	-	4	-	32	MHz
$I_{DD}^{(4)}$	HSE current consumption	During startup	-	-	5.5	mA
		$V_{CC}=3\text{ V}, R_m=30\ \Omega,$ $C_L=10\text{ pF}@8\text{ MHz}$ $HSE\_DRV[1:0]=01$	-	0.58	-	
		$V_{CC}=3\text{ V}, R_m=30\ \Omega,$ $C_L=5\text{ pF}@16\text{ MHz}$ $HSE\_DRV[1:0]=10$	-	0.89	-	
		$V_{CC}=3\text{ V}, R_m=30\ \Omega,$ $C_L=10\text{ pF}@24\text{ MHz}$ $HSE\_DRV[1:0]=10/11$	-	1.14	-	
$t_{SU(HSE)}^{(3)(4)}$	Startup Time	$f_{OSC\_IN}=32\text{ MHz}$ $HSE\_STARTUP[1:0]=00$ $HSE\_DRV[1:0]=11$	-	2	-	ms
		$f_{OSC\_IN}=4\text{ MHz}$ $HSE\_STARTUP[1:0]=00$ $HSE\_DRV[1:0]=11$	-	2	-	

1. Crystal/ceramic resonator characteristics are based on the manufacturer's datasheet.
2. Guaranteed by design, not tested in production.
3.  $t_{SU(HSE)}$  is the startup time from enable (by software) to when the clock oscillation reaches a stable state , measured for a standard crystal/resonator, which can vary considerably from one crystal/resonator to another .
4. Data is based on assessment results and is not tested in production.

### 5.3.6.4. External low speed crystal

The low-speed external (LSE) clock can be supplied with a 32.768 KHz crystal resonator oscillator. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time.

Table 5-14 External low-speed crystal feature

Symbol	Parameter	Condition <sup>(1)</sup>	Minimum <sup>(2)</sup>	Typical	Maximum <sup>(2)</sup>	Unit
I <sub>DD</sub> <sup>(4)</sup>	LSE current consumption	LSE_DRIVER [1:0] = 00	-	250	-	nA
		LSE_DRIVER [1:0] = 01	-	560	-	
		LSE_DRIVER [1:0] = 10	-	920	-	
		LSE_DRIVER[1:0] = 11	-	1260	-	
t <sub>SU(LSE)</sub> <sup>(3)(4)</sup>	Startup Time	-	-	3	-	s

- Crystal/ceramic resonator characteristics are based on the manufacturer's datasheet.
- Guaranteed by design, not tested in production.
- t<sub>SU(LSE)</sub> is the startup time from enable (by software) to when the clock oscillation reaches a stable, measured for a standard crystal/resonator, which may vary greatly from crystal to resonator.
- Data is based on assessment results and is not tested in production.

### 5.3.7. Internal high frequency clock source HSI characteristics

Table 5-15 Internal high frequency clock source characteristics

Symbol	Parameter	Condition	Minimum	Typical	Maximum	Unit
f <sub>HSI</sub>	HSI frequency	-	-	4.0 8.0 16.0 22.12 24.0	-	MHz
ΔT <sub>emp (HSI)</sub>	HSI frequency temperature drift	V <sub>CC</sub> = 1.7 to 5.5 V, T <sub>A</sub> = 25 °C	-1 <sup>(2)</sup>	-	1 <sup>(2)</sup>	%
		V <sub>CC</sub> = 1.7 to 5.5 V, T <sub>A</sub> = 0 to 85 °C	-2 <sup>(2)</sup>	-	2 <sup>(2)</sup>	
		V <sub>CC</sub> = 1.7 to 5.5 V, T <sub>A</sub> = -40 to 85 °C	-4 <sup>(2)</sup>	-	2 <sup>(2)</sup>	
		V <sub>CC</sub> = 1.7 to 5.5 V, T <sub>A</sub> = -40 to 105 °C	-4 <sup>(2)</sup>	-	4 <sup>(2)</sup>	
f <sub>TRIM</sub> <sup>(1)</sup>	HSI fine-tuning accuracy	-	-	0.1	-	%
ΔT <sub>emp(HSI)</sub>	HSI frequency temperature drift	-	45 <sup>(1)</sup>	-	55 <sup>(1)</sup>	%
t <sub>stab (HSI)</sub>	HSI stabilization time	-	-	2	4 <sup>(1)</sup>	us
f <sub>TRIM</sub> <sup>(1)</sup>	HSI fine-tuning accuracy	4 MHz	-	110	-	uA
		8 MHz	-	120	-	
		16 MHz	-	170	-	
		22.12 MHz, 24 MHz	-	210	-	

- Guaranteed by design, not tested in production.
- Data is based on assessment results and is not tested in production.

### 5.3.8. Internal low frequency clock source LSI characteristics

Table 5-16 Internal low frequency clock characteristics

Symbol	Parameter	Condition	Minimum	Typical	Maximum	Unit
$f_{LSI}$	LSI frequency	-	-	32.768	-	KHz
$\Delta T_{emp(LSI)}$	LSI frequency temperature drift	$V_{CC} = 3.3 V$ , $T_A = 25 ^\circ C$	-3	-	+3	%
		$V_{CC} = 1.7 \text{ to } 5.5 V$ , $T_A = 0 \text{ to } 85 ^\circ C$	-10 <sup>(2)</sup>	-	10 <sup>(2)</sup>	
		$V_{CC}=1.7 \sim 5.5 V$ , $T_A= 0 \sim 105 ^\circ C$	- 15 <sup>(2)</sup>	-	15 <sup>(2)</sup>	
		$V_{CC} = 1.7 \sim 5.5 V$ , $T_A = -40 \text{ to } 105 ^\circ C$	-20 <sup>(2)</sup>	-	20 <sup>(2)</sup>	
$f_{TRIM}^{(1)}$	LSI fine-tuning accuracy	-	-	0.2	-	%
$t_{Stab(LSI)}^{(1)}$	LSI stabilization time	-	-	150	-	us
$I_{DD(LSI)}^{(1)}$	LSI current consumption	-	-	210	-	nA

1. Guaranteed by design, not tested in production.
2. Data is based on assessment results and is not tested in production.

### 5.3.9. Phase locked loop (PLL) characteristics

Table 5-17 Phase locked loop characteristics

Symbol	Parameter	Condition	Minimum	Typical	Maximum	Unit
$f_{PLL\_IN}$	Input frequency	$T_A = 25 ^\circ C$ , $V_{CC} = 3.3 V$ PLL * 2	16 <sup>(1)</sup>	-	24 <sup>(1)</sup>	MHz
		$T_A = 25 ^\circ C$ , $V_{CC} = 3.3 V$ PLL * 3	22.12 <sup>(1)</sup>	-	24 <sup>(1)</sup>	
$f_{PLL\_OUT}$	Output frequency	$T_A = 25 ^\circ C$ , $V_{CC} = 3.3 V$	32 <sup>(1)</sup>	-	72	MHz
Jitter	Period jitter	-	-	-	0.3 <sup>(1)</sup>	ns
$t_{LOCK}$	Latch time	$f_{PLL\_IN} = 24 \text{ MHz}$	-	15	40 <sup>(1)</sup>	us

1. Guaranteed by design, not tested in production.

### 5.3.10. Memory characteristics

Table 5-18 Memory characteristics

Symbol	Parameter	Condition	Typical	Maximum <sup>(1)</sup>	Unit
$t_{prog}$	Page program	-	1.0	1.5	ms
$t_{ERASE}$	Page/sector/mass erase	-	3.0	4.5	ms
$I_{DD}$	Page programme	-	2.1	2.9	mA
	Page/sector/mass erase	-	2.1	2.9	mA

1. Guaranteed by design, not tested in production.

Table 5-19 Memory erase times and data retention

Symbol	Parameter	Condition	Minimum <sup>(1)</sup>	Unit
$N_{END}$	Erase and write times	$T_A = -40 \sim 85 ^\circ C$	100	kcycle

		$T_A = 85 \sim 105 \text{ }^\circ\text{C}$	10	
$t_{RET}$	Data retention period	10 Kcycle $T_A = 55 \text{ }^\circ\text{C}$	20	Year

1. Data is based on assessment results and is not tested in production.

### 5.3.11. EFT characteristics

Table 5-20 EFT characteristics

Symbol	Parameter	Condition	Grade	Typical	Unit
EFT to Power	-	IEC61000-4-4	A	A	kV

### 5.3.12. ESD & LU characteristics

Table 5-21 ESD & LU characteristics

Symbol	Parameter	Condition	Typical	Unit
$V_{ESD(HBM)}$	Static discharge voltage (human body model)	ESDA/JEDEC JS-001-2017	6	KV
$V_{ESD(CDM)}$	Static discharge voltage (charging equipment model)	ESDA/JEDEC JS-002-2018	1	KV
$V_{ESD(MM)}$	Static discharge voltage ( machine model)	JESD22-A115C	200	V
LU	Static latch-up	JESD78E	200	mA

### 5.3.13. Port characteristics

Table 5-22 IO static characteristics

Symbol	Parameter	Condition	Minimum	Typical	Maximum	Unit
$V_{IH}$	Input high level voltage	$V_{CC} = 1.7 \text{ to } 5.5 \text{ V}$	$0.7V_{CC}$	-	-	V
$V_{IL}$	Input low level voltage	$V_{CC} = 1.7 \text{ to } 5.5 \text{ V}$	-	-	$0.3V_{CC}$	V
$V_{hys}^{(1)}$	Schmitt hysteresis voltage	-	-	200	-	mV
$I_{Ikg}$	Input leakage current	-	-	-	1	$\mu\text{A}$
$R_{PU}$	Pull-up resistor	-	30	50	70	$\text{k}\Omega$
$R_{PD}$	Pull-down resistor	-	30	50	70	$\text{k}\Omega$
$C_{IO}^{(1)}$	Pin capacitance	-	-	5	-	pF

1. Guaranteed by design, not tested in production.

Table 5-23 Output voltage characteristics

Symbol	Parameters <sup>(1)</sup>	Condition	Minimum	Maximum	Unit	
$V_{OL}^{(2)}$	COM IO output low level	GPIOx_OSPEED R=11	$I_{OL} = 8 \text{ mA}, V_{CC} \geq 2.7 \text{ V}$	-	0.4	V
			$I_{OL} = 4 \text{ mA}, V_{CC} = 1.8 \text{ V}$	-	0.5	
$V_{OH}^{(2)}$	COM IO output high level	GPIOx_OSPEED R=11	$I_{OH} = 8 \text{ mA}, V_{CC} \geq 2.7 \text{ V}$	$V_{CC} - 0.4$	-	V
			$I_{OH} = 4 \text{ mA}, V_{CC} = 1.8 \text{ V}$	$V_{CC} - 0.5$	-	



1. IO types can refer to the terms and symbols defined by the pins.
2. Data is based on assessment results and is not tested in production.

### 5.3.14. NRST pin characteristics

Table 5-24 NRST pin characteristics

Symbol	Parameter	Condition	Minimum	Typical	Maximum	Unit
$V_{IH}$	Input high level voltage	$V_{CC} = 1.7$ to $5.5$ V	$0.7V_{CC}$	-	-	V
$V_{IL}$	Input low level voltage	$V_{CC} = 1.7$ to $5.5$ V	-	-	$0.2V_{CC}$	V
$V_{hys}^{(1)}$	Schmitt hysteresis voltage	-	-	300	-	mV
$I_{lkg}$	Input leakage current	-	-	-	1	uA
RPU <sup>(1)</sup>	Pull-up resistor	-	30	50	70	kΩ
RPD <sup>(1)</sup>	Pull-down resistor	-	30	50	70	kΩ
$C_{IO}$	Pin capacitance	-	-	5	-	pF

1. Guaranteed by design, not tested in production.

### 5.3.15. ADC characteristics

Table 5-25 ADC characteristics

Symbol	Parameter	Condition	Minimum	Typical	Maximum	Unit
$V_{CCA}$	Analog supply voltage for ADC ON	-	2.0	-	5.5	V
$I_{CCA}$	Current consumption	@1 MSPS	-	0.4	-	mA
$C_{IN}^{(1)}$	Internal sample and hold capacitors	-	-	5	8	pF
$f_{ADC}$	Convert clock frequency	$V_{CCA}=2.0 \sim 2.3$ V	0.8	4	8 <sup>(2)</sup>	MHz
		$V_{CCA}=2.3 \sim 5.5$ V	0.8	8	16 <sup>(2)</sup>	MHz
$t_{smp}^{(1)}$	Sampling time	$f_{ADC}=16$ MHz	0.219	-	14.97	us
		$V_{CCA}=2.0 \sim 5.5$ V	3.5	-	239.5	$1/f_{ADC}$ C
$t_{smp\_setup}^{(1)}$	Sampling setup time ( $V_{REFINT}$ , $V_{CCA}/3$ , OPA 1~3, DAC 1~2)	-	15	-	-	μs
$t_{conv}^{(1)}$	Total conversion time	$V_{CCA}=2.0 \sim 5.5$ V	-	12	-	$1/f_{ADC}$ C
$t_{eoc}^{(1)}$	Conversion end time	$V_{CCA}=2.0 \sim 5.5$ V	-	0.5	-	$1/f_{ADC}$ C
DNL <sup>(2)</sup>	Differential linearity error	-	-	± 1	-1 ~ 1.5	LSB
INL <sup>(2)</sup>	Integral linearity error	-	-	-	± 3	LSB
Offset <sup>(2)</sup>	Offset error	-	-	± 1.5	± 3	LSB

1. Guaranteed by design, not tested in production.
2. Data is based on assessment results and is not tested in production.

## 5.3.16. DAC characteristics

Table 5-26 DAC characteristics

Symbol	Parameter	Comments	Minimum	Typical	Maximum	Unit
$V_{CCA}$	Analog supply voltage for DAC ON	Buffer ON	2.2	-	5.5	V
		Buffer OFF	2.2	-	5.5	V
$R_{LOAD}^{(1)}$	Resistive load	$V_{SSA}$ with buffer ON	5	-	-	k $\Omega$
		$V_{CCA}$ with buffer ON	15	-	-	k $\Omega$
$R_O^{(1)}$	Impedance output	The minimum resistive load between DAC_VOUT and $V_{SSA}$ to have a 1% accuracy is 1.5 M $\Omega$ (When the buffer is ON) .	-	-	15	k $\Omega$
$C_{LOAD}^{(1)}$	Capacitive load	Maximum capacitive load at DAC_OUT pin (When the buffer is ON).	-	-	50	pF
$DAC\_OUT_{min}^{(1)}$	Lower DAC_OUT voltage	Buffer ON,it gives the maximum output excursion of the DAC.	0.2	-	-	V
$DAC\_OUT_{max}^{(1)}$	Higher DAC_OUT voltage		-	-	$V_{CCA} - 0.2$	V
$DAC\_OUT_{min}^{(1)}$	Lower DAC_OUT voltage	Buffer OFF,it gives the maximum output excursion of the DAC.	-	0.5	-	mV
$DAC\_OUT_{max}^{(1)}$	Higher DAC_OUT voltage		-	-	$V_{CCA} - 10\text{ mV}$	V
$I_{CCA}^{(1)}$	$V_{CCA}$ consumption <sup>(2)</sup>	With no load, middle code (0x800) on the inputs	-	-	600	$\mu\text{A}$
		With no load, worst code (0xF1C) at $V_{CCA} = 3.6\text{ V}$ in terms of DC consumption on the inputs	-	-	700	
$DNL^{(2)}$	Differential linearity error	Given for the DAC in 10 bits configuration	-	-	$\pm 1$	LSB
		Given for the DAC in 12 bits configuration	-	-	$\pm 3$	
$INL^{(2)}$	Integral linearity error	Given for the DAC in 10 bits configuration	-	-	$\pm 1$	LSB
		Given for the DAC in 12 bits configuration	-	-	$\pm 4$	
Offset <sup>(2)</sup>	offset error	Given for the DAC in 10 bits	-	-	$\pm 3$	LSB
		Given for the DAC in 12 bits	-	-	$\pm 12$	
Gain error <sup>(2)</sup>	Gain error	Given for the DAC in 12 bits configuration	-	-	$\pm 0.5$	%
$t_{SETTLING}^{(2)}$	Settling time	$C_{LOAD} \leq 50\text{ pF}$ , $R_{LOAD} \geq 5\text{ k}\Omega$ Full scale: for a 10 bits input code transition between the lowest and the highest input codes when DAC_OUT reaches final value $\pm 1\text{LSB}$	-	4	10	$\mu\text{s}$
Update rate <sup>(2)</sup>	Max frequency for a correct DAC_OUT change when small variation in the inputcode (from code i to i+1LSB)	$C_{LOAD} \leq 50\text{ pF}$ , $R_{LOAD} \geq 5\text{ k}\Omega$	-	-	1	MS/s
$t_{WAKEUP}^{(2)}$	Wakeup time from off state	$C_{LOAD} \leq 50\text{ pF}$ , $R_{LOAD} \geq 5\text{ k}\Omega$ Input code between lowest and highest possible ones.	-	6.5	10	$\mu\text{s}$
$P_{SRR+}^{(1)}$	Power supply rejection ratio (to $V_{CCA}$ ) (static DC measurement)	No $R_{LOAD}$ , $C_{LOAD} = 50\text{ pF}$	-	-67	-40	dB

1. Guaranteed by design, not tested in production.
2. Data is based on assessment results and is not tested in production.

### 5.3.17. Comparator characteristics

Table 5-27 Comparator characteristics<sup>(1)</sup>

Symbol	Parameter	Condition	Minimum	Typical	Maximum	Unit	
V <sub>IN</sub>	Input voltage range	-	0	-	V <sub>CC</sub>	V	
V <sub>SC</sub>	Scaler offset voltage	-	-	±5	± 10	mV	
I <sub>CCA(SCALER)</sub>	Scaler static consumption	-	-	0.8	1	uA	
t <sub>START_SCALER</sub>	Scaler startup time	-	-	100	200	us	
t <sub>START</sub>	Startup time	High-speed mode	-	-	5	us	
		Medium-speed mode	-	-	15		
t <sub>D</sub>	Propagation delay	High-speed mode	200 mV step, 100 mV overdrive	-	40	70	ns
		Medium-speed mode		-	0.9	2.3	us
		High-speed mode	>200 mV step, 100 mV overdrive	-	-	85	ns
		Medium-speed mode		-	-	3.4	us
V <sub>offset</sub>	Offset error	-	-	±5	-	mV	
V <sub>hys</sub>	Hysteresis	No hysteresis	-	0	-	mV	
		With hysteresis	-	20	-		
I <sub>CCA</sub>	Consumption	High-speed mode	Static	-	250	-	uA
			With 50 KHz and ±100 mv overdrive square signal	-	250	--	uA
		Medium-speed mode	Static	-	7	-	uA
			With 50 KHz and ±100 mv overdrive square signal	-	8	-	uA

1. Guaranteed by design, not tested in production.

### 5.3.18. Operational amplifier characteristics

Table 5-28 Comparator characteristics

Symbol	Parameter	Condition	Minimum	Typical	Maximum	Unit
V <sub>i</sub>	Input voltage	-	0	-	V <sub>CCA</sub>	V
V <sub>o</sub>	The output voltage	-	0.1	-	V <sub>CC</sub> - 0.2	V
I <sub>o</sub>	Output current	-	-	-	2.2	mA
R <sub>L</sub>	load time	-	5	-	-	kΩ
t <sub>start</sub>	initialization time	-	-	-	20	us
V <sub>io</sub>	Input offset voltage	-	--	±6	-	mV
PM	Phase margin	-	-	80	-	Deg
UGBW	unity gain width	-	-	10	-	MHz
SR	Slew rate	-	-	8	-	V/us

### 5.3.19. Temperature sensor characteristics

Table 5-29 Temperature sensor characteristics

Symbol	Parameter	Minimum	Typical	Maximum	Unit
$T_L^{(1)}$	$V_{TS}$ linearity with temperature	-	$\pm 1$	$\pm 2$	$^{\circ}\text{C}$
Avg_Slope <sup>(1)</sup>	Average slope	2.3	2.5	2.7	mV/ $^{\circ}\text{C}$
$V_{30}$	Voltage at 30 $^{\circ}\text{C}$ ( $\pm 5$ $^{\circ}\text{C}$ )	0.742	0.76	0.785	V
$t_{\text{START}}^{(1)}$	Start up time entering in continuous mode	-	70	120	us
$t_{\text{s\_setup}}^{(1)}$	ADC sampling time when reading the temperature	15	-	-	us

1. Guaranteed by design, not tested in production.
2. Data is based on assessment results and is not tested in production.

### 5.3.20. LCD Controller Characteristics

Table 5-30 LCD Controller Characteristics

Symbol	Parameter	Condition	Minimum	Typical	Maximum	Unit
$I_{\text{LCD}}^{(1)(3)}$	LCD supply current	External low drive resistive mode	-	0.6	-	$\mu\text{A}$
		Internal low drive resistive mode	-	4	-	
		Internal high drive resistive mode	-	10	-	
$R_H^{(2)}$	Low drive resistive	-	-	1080	-	k $\Omega$
$R_L^{(2)}$	High drive resistive	-	-	360	-	
$V_{\text{LCDH}}$	LCD adjustable highest level voltage	-	-	$V_{\text{CCA}}$	-	V
$V_{\text{LCD3}}$	LCD highest level voltage	-	-	$V_{\text{LCDH}}$	-	
$V_{\text{LCD2}}$	LCD 2/3 level voltage	-	-	$2/3 V_{\text{LCDH}}$	-	
$V_{\text{LCD1}}$	LCD 1/3 level voltage	-	-	$1/3 V_{\text{LCDH}}$	-	
$V_{\text{LCD0}}$	LCD lowest level voltage	-	-	$V_{\text{SS}}$	-	
$\Delta V_{\text{LCD}}^{(3)}$	LCD segment/common level voltage error	$T_A = -40 \sim 105$ $^{\circ}\text{C}$	-	-	$\pm 50$	mV

1. LCD enabled with  $V_{\text{CCA}}=3.3$  V, 1/4 duty, 1/3 bias, scan frequency 256 Hz, all pixels active, no LCD connected.
2. Guaranteed by design, not tested in production.
3. Data is based on assessment results and is not tested in production.

### 5.3.21. Built-in reference voltage characteristics

Table 5-31 Built-in reference voltage ( $V_{\text{REFBUF}}$ ) characteristics

Symbol	Parameter	Condition	Minimum	Typical	Maximum	Unit
$V_{\text{REFINT}}$	Internal reference voltage	-	1.17	1.2	1.23	V

Symbol	Parameter	Condition	Minimum	Typical	Maximum	Unit
$t_{start\_VREFINT}$	Start time of $V_{REFINT}$	-	-	10	15	us
$T_{coeff\_VREFINT}$	Temperature coefficient of $V_{REFINT}$	-	-	-	100 <sup>(1)</sup>	ppm/°C
$I_{VCC}$	Current consumption from $V_{CC}$	-	-	12	20	uA

1. Guaranteed by design, not tested in production.

### 5.3.22. ADC Built-in reference voltage characteristics

Table 5-32 ADC Built-in reference voltage ( $V_{REFBUF}$ ) characteristics<sup>(1)</sup>

Symbol	Parameter	Condition	Minimum	Typical	Maximum	Unit
$V_{REFBUF26}$	Internal 2.66 V reference voltage	$T_A=25\text{ }^\circ\text{C}$ , $V_{CCA}=3.3\text{ V}$	3.63	2.66	2.69	V
$V_{REFBUF20}$	Internal 2.14 V reference voltage	$T_A=25\text{ }^\circ\text{C}$ , $V_{CCA}=3.3\text{ V}$	2.12	2.14	2.16	V
$t_{start\_VREFBUF}$	Start time of $V_{REFBUF}$	-	-	-	2	μs
$T_{coeff\_VREF-BUF}$	Temperature coefficient of $V_{REFBUF}$	$T_A=-40\text{ }^\circ\text{C} \sim 105\text{ }^\circ\text{C}$	-	-	120	ppm/°C

1. Guaranteed by design, not tested in production.

### 5.3.23. Timer characteristics

Table 5-33 Timer characteristics

Symbol	Parameter	Condition	Minimum	Maximum	Unit
$t_{res(TIM)}$	Timer resolution time	-	1	-	$t_{TIMxCLK}$
		$f_{TIMxCLK} = 72\text{ MHz}$	13.889	-	ns
$f_{EXT}$	Timer external clock frequency on CH1 to CH4	-	-	$f_{TIMxCLK}/2$	MHz
		$f_{TIMxCLK} = 72\text{ MHz}$	-	24	
$Res_{TIM}$	Timer resolution	TIM1/3/14/15/16/17	-	16	Bit
$t_{COUNTER}$	16 bits counter clock period	-	1	65536	$t_{TIMxCLK}$
		$f_{TIMxCLK} = 72\text{ MHz}$	0.013889	913	us

Table 5-34LPTIM characteristics (clock selection LSI)

Prescaler	PRESC[2:0]	Minimum overflow	Maximum overflow	Unit
/1	0	0.0305	1998.848	ms
/2	1	0.0610	3997.696	
/4	2	0.1221	8001.9456	
/8	3	0.2441	15997.3376	
/16	4	0.4883	32001.2288	
/32	5	0.9766	64002.4576	
/64	6	1.9531	127998.3616	
/128	7	3.9063	256003.2768	

Table 5-35 IWDG characteristics (clock selection LSI)

Prescaler	PR[2:0]	Minimum overflow	Maximum overflow	Unit
/4	0	0.122	499.712	ms
/8	1	0.244	999.424	
/16	2	0.488	1998.848	
/32	3	0.976	3997.696	
/64	4	1.952	7995.392	
/128	5	3.904	15990.784	
/256	6 or 7	7.808	31981.568	

Table 5-36 WWDG characteristics (Clock selection 48 MHz PCLK)

Prescaler	WDGTB[1:0]	Minimum overflow	Maximum overflow	Unit
1*4096	0	0.085	5.461	ms
2*4096	1	0.171	10.923	
4*4096	2	0.341	21.845	
8*4096	3	0.683	43.691	

### 5.3.24. Communication port characteristics

#### 5.3.24.1. I<sup>2</sup>C bus interface features

The I<sup>2</sup>C interface meets the timing requirements of the I<sup>2</sup>C-bus specification and user manual:

- Standard-mode (Sm): 100 kbit/s
- Fast-mode (Fm): 400 kbit/s

The I<sup>2</sup>C timings requirements is guaranteed by design, provided the I<sup>2</sup>C peripheral is properly configured and the I<sup>2</sup>C CLK frequency is greater than the minimum required in the table below.

Table 5-37 Minimum I<sup>2</sup>C CLK frequency

Symbol	Parameter	Condition	Minimum	Unit
f <sub>I2CCLK(min)</sub>	Minimum I <sup>2</sup> C CLK frequency	Standard-mode	2	MHz
		Fast-mode	9	

I<sup>2</sup>C SDA and SCL pins have analogue filtering, see table below.

Table 5-38 I<sup>2</sup>C filter characteristics

Symbol	Parameter	Minimum	Maximum	Unit
t <sub>AF</sub>	Limiting duration of spikes suppressed by the filter (spikes shorter than the limiting duration are suppressed)	50	260	ns

#### 5.3.24.2. Serial peripheral interface (SPI) characteristics

Table 5-39 SPI characteristics

Symbol	Parameter	Condition	Minimum	Maximum	Unit
f <sub>SCK</sub>	SPI clock frequency	Master mode	-	24	MHz

Symbol	Parameter	Condition	Minimum	Maximum	Unit
$1/t_c(\text{SCK})$		Slave mode	-	18	
$t_{r(\text{SCK})}$ $t_{f(\text{SCK})}$	SPI clock rise and fall time	Capacitive load: C = 15 pF	-	6	ns
$t_{su(\text{NSS})}$	NSS setup time	Slave mode	$2 T_{\text{pclk}}$	-	ns
$t_{h(\text{NSS})}$	NSS hold time	Slave mode	$2 T_{\text{pclk}}$	-	ns
$t_w(\text{SCKH})$ $t_w(\text{SCKL})$	SCK high and low time	Master mode, presc = 2	$T_{\text{pclk}} - 2$	$T_{\text{pclk}} + 1$	ns
$t_{su(\text{MI})}$ $t_{su(\text{SI})}$	Data input setup time	Master mode	1	-	ns
		Slave mode	3	-	
$t_{h(\text{MI})}$	Data input hold time	Master mode	5	-	ns
$t_{h(\text{SI})}$		Slave mode	2	-	
$t_a(\text{SO})$	Data output access time	Slave mode	0	$3 T_{\text{pclk}}$	ns
$t_{dis(\text{SO})}$	Data output disable time	Slave mode	$2 T_{\text{pclk}}$	-	ns
$t_v(\text{SO})$	Data output valid time	Slave mode(after enable edge)	0	20	ns
$t_v(\text{MO})$	Data output valid time	Master mode(after enable edge)	-	5	ns
$t_h(\text{SO})$	Data output hold time	Slave mode(after enable edge)	2	-	ns
$t_h(\text{MO})$		Master mode(after enable edge)	1	-	
DuCy(SCK)	SPI slave input clock duty cycle	Slave mode	45	55	%

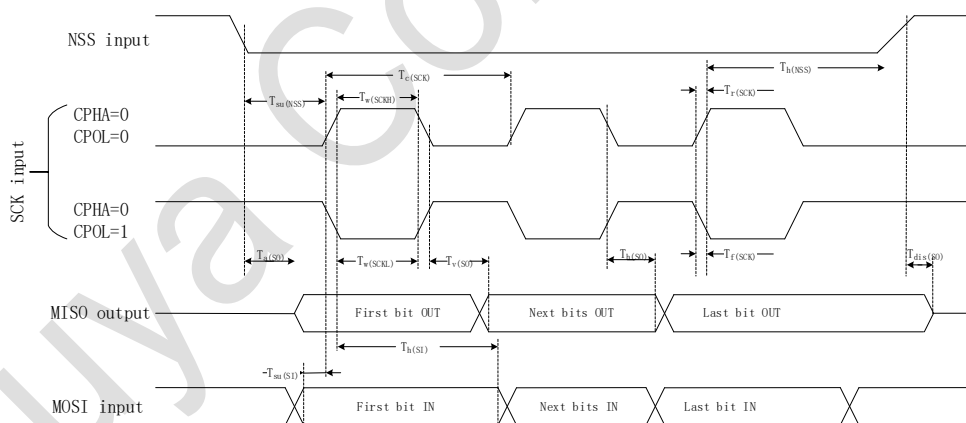


Figure 5-3 SPI timing diagram – Slave mode and CPHA=0

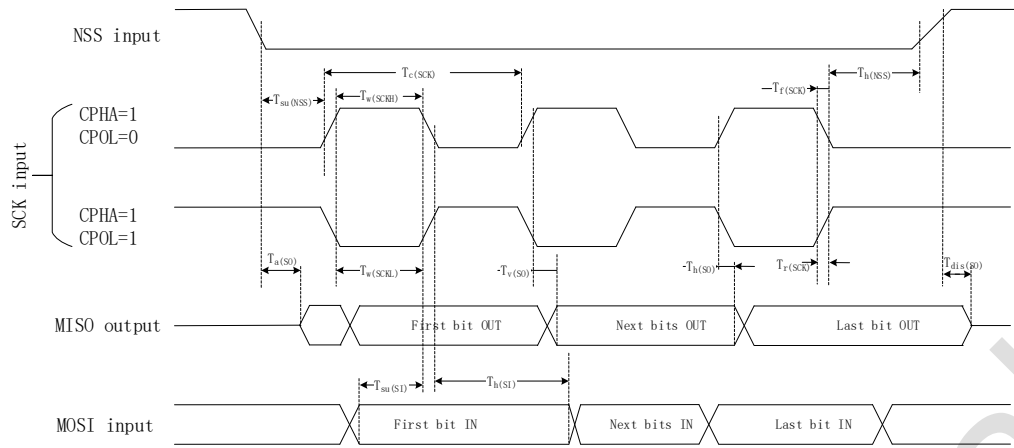


Figure 5-4 SPI timing diagram – Slave mode and CPHA=1

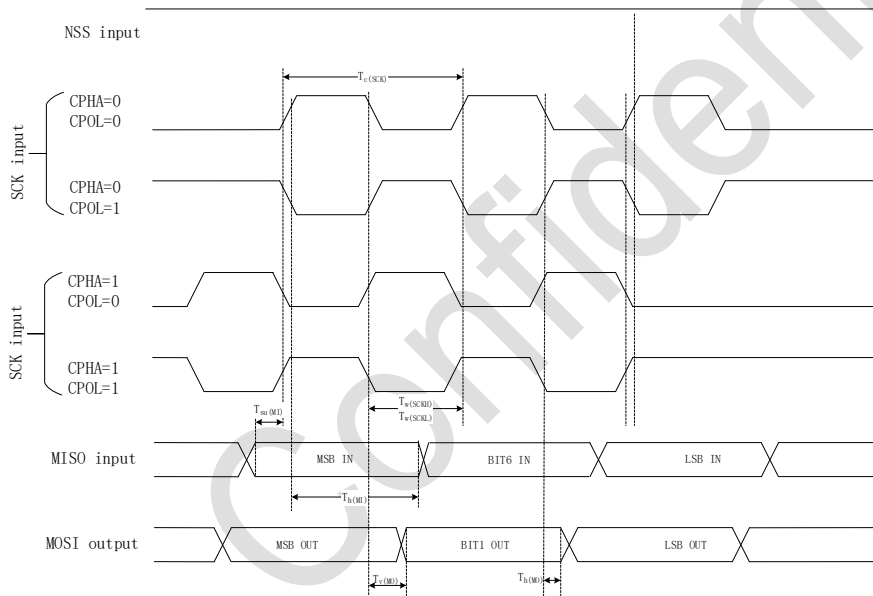
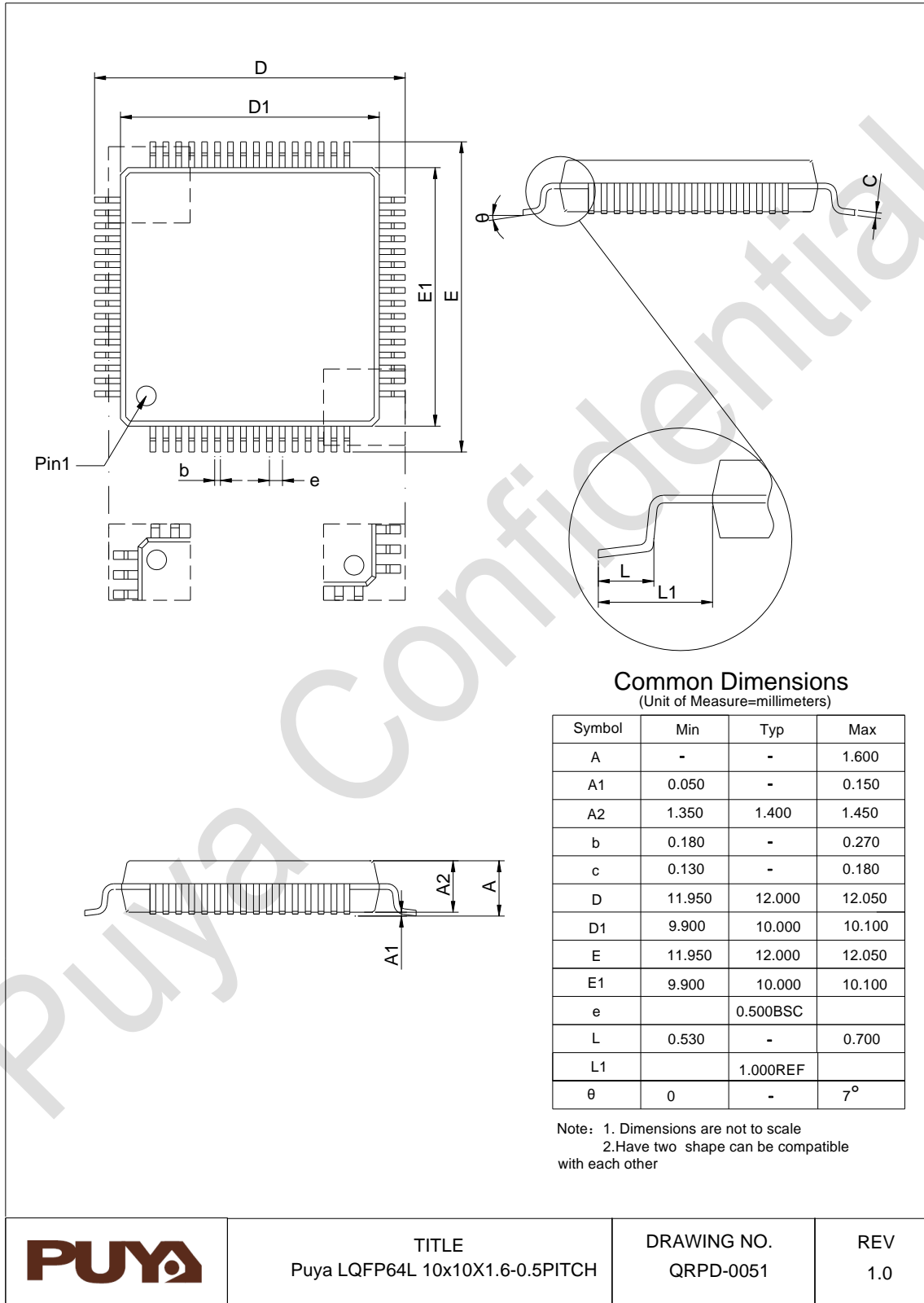


Figure 5-5 SPI timing diagram – Master mode



## 6. Package Information

### 6.1. LQFP64 package size

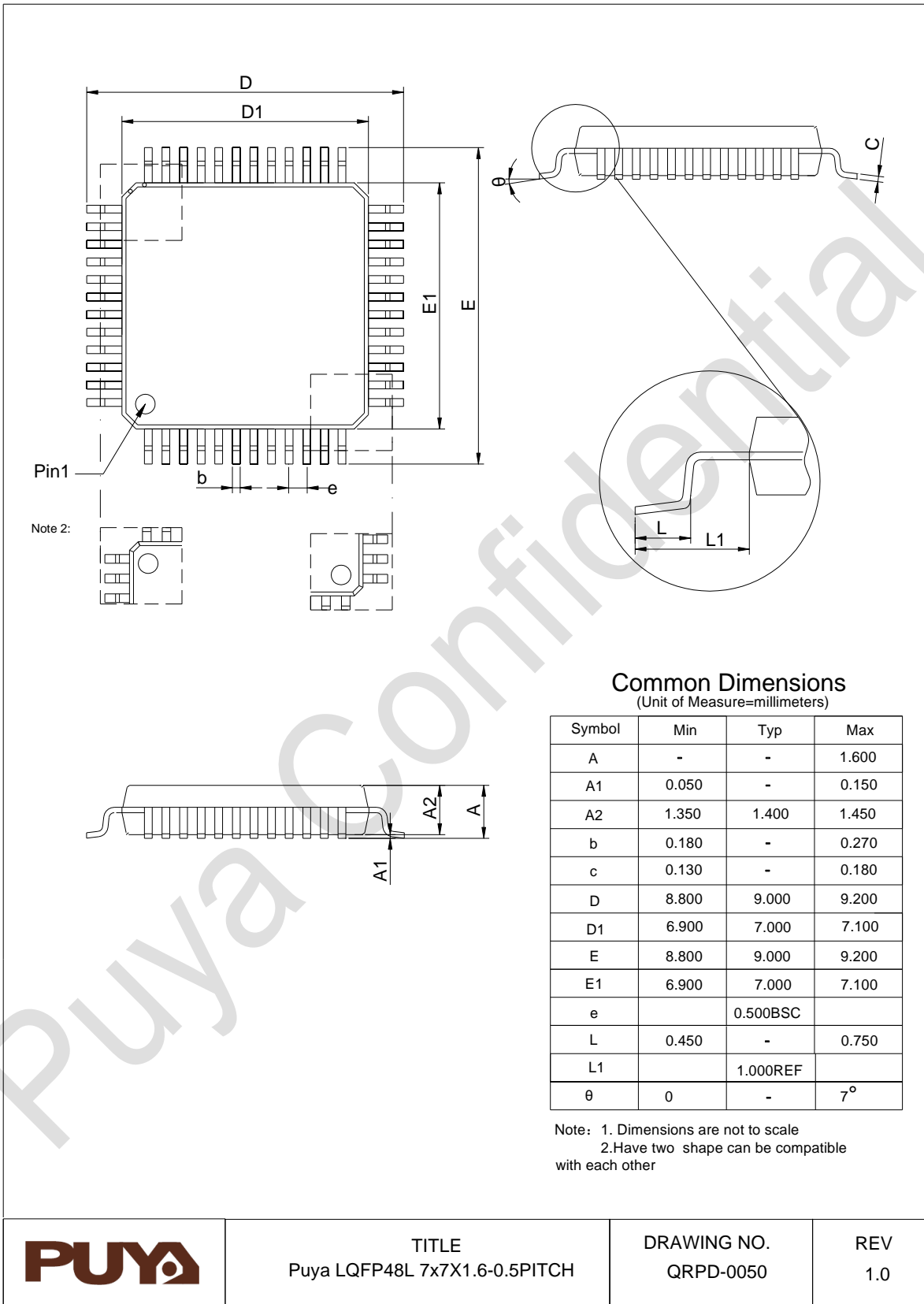



TITLE  
Puya LQFP64L 10x10X1.6-0.5PITCH

DRAWING NO.  
QRPD-0051

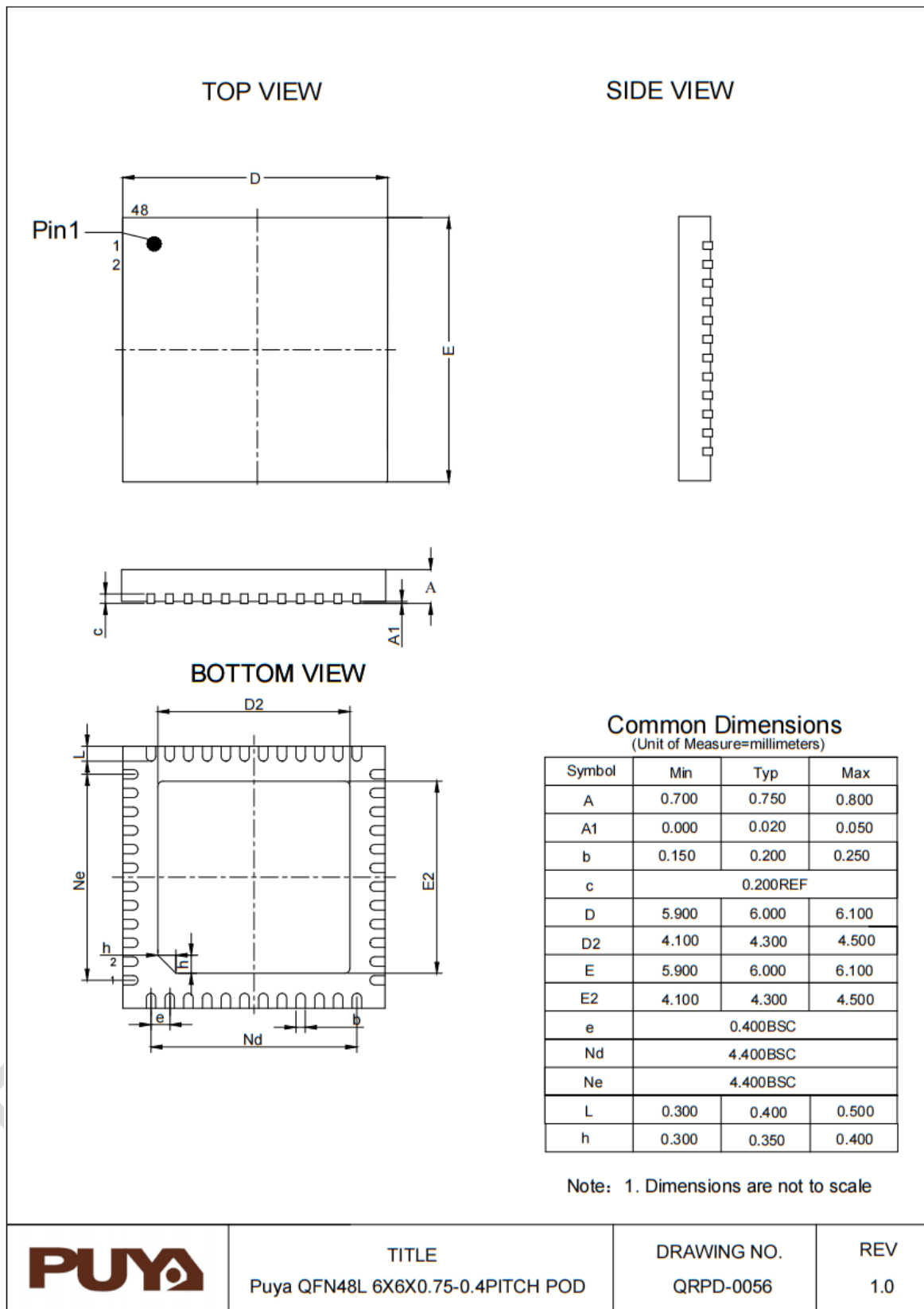
REV  
1.0

## 6.2. LQFP48 package size

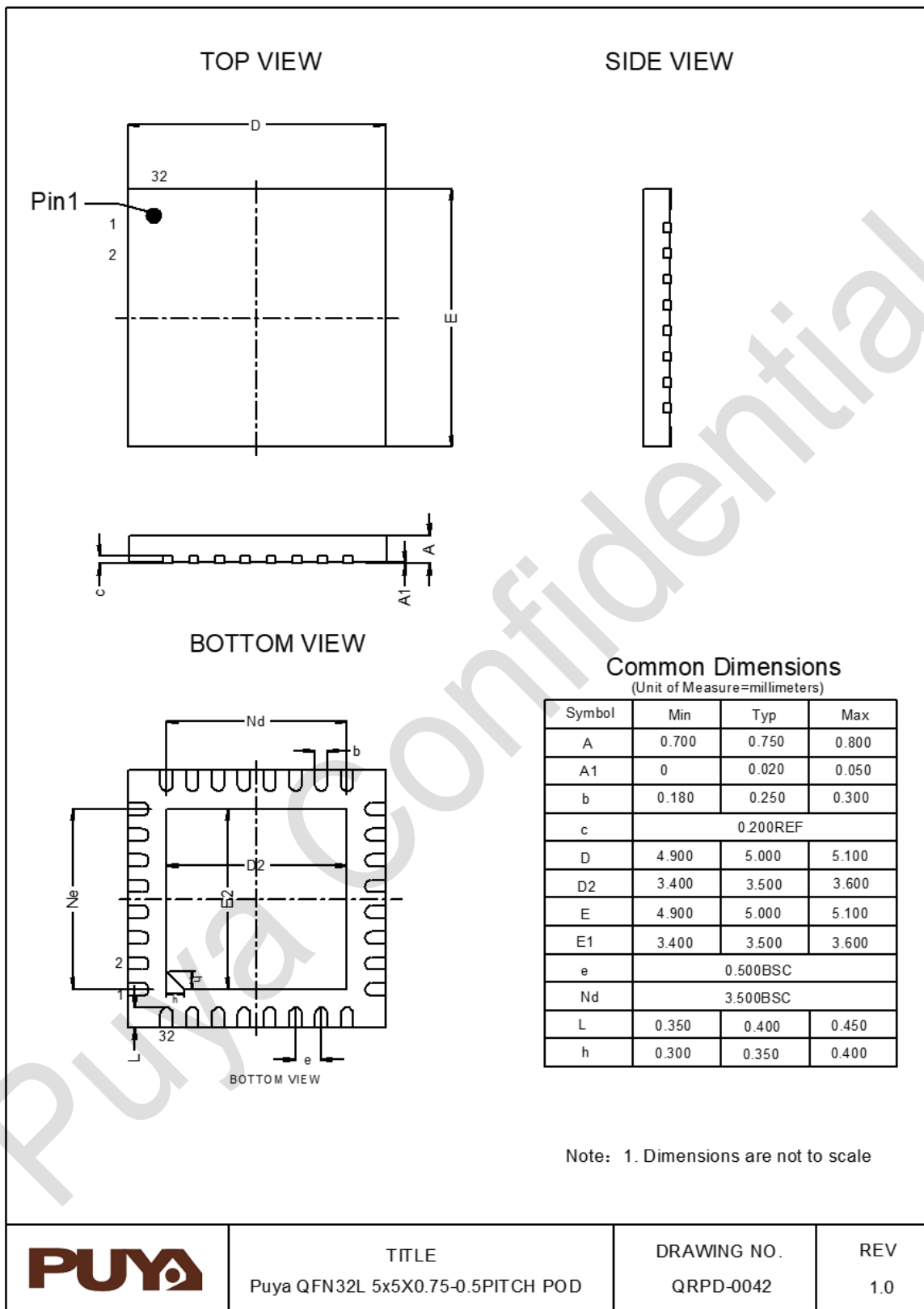


	<p>TITLE Puya LQFP48L 7x7X1.6-0.5PITCH</p>	<p>DRAWING NO. QRPD-0050</p>	<p>REV 1.0</p>
---	--	----------------------------------	--------------------

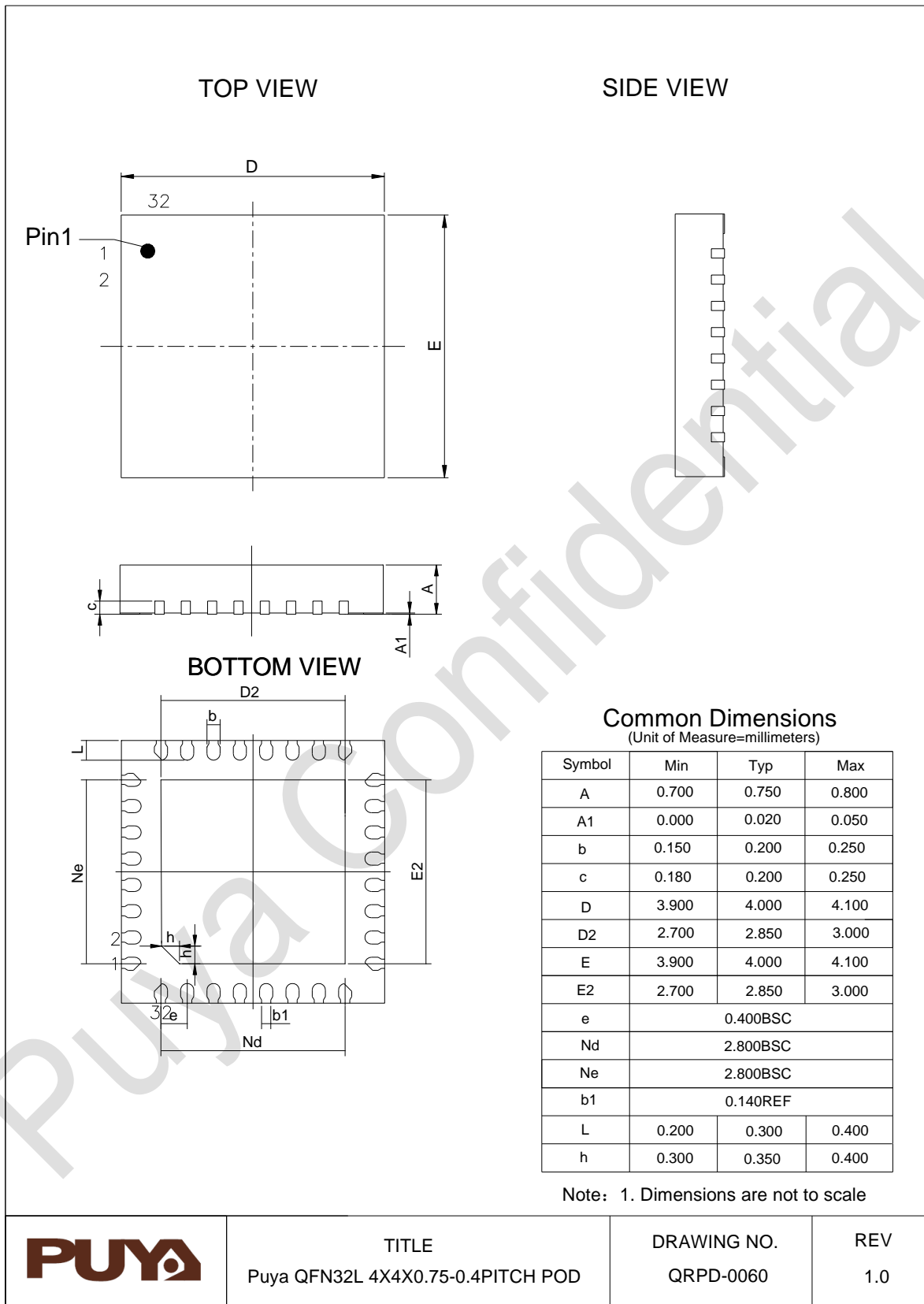
### 6.3. QFN48 package size



### 6.4. QFN32(5\*5) package size



### 6.5. QFN32(4\*4) package size



## 7. Ordering Information

	PY	32	F	072	R1	8	T	6	x
<u>Company</u>									
<u>Product family</u> ARM <sup>®</sup> based 32-bit microcontroller									
<u>Product type</u> F = General purpose									
<u>Sub-family</u> 072 = PY32F072xx									
<u>Pin count</u>									
R1 = 64 pins Pinout1 C1 = 48 pins Pinout1 K1 = 32 pins Pinout1 K3 = 32 pins Pinout3									
<u>User code memory size</u> B = 128 Kbytes									
<u>Package</u> U = QFN T = LQFP									
<u>Temperature range</u> 6 = -40 °C to + 85 °C 7 = -40 °C to + 105 °C									
<u>Options</u> xxx = code ID of programmed parts(includes packing type) TR = tape and reel packing TU = Tube Packing blank = tray packing									

## 8. Version History

Version	Date	Updated record
V1.0	2023.08.31	1. Initial version
V1.1	2024.01.16	1. Updated Table 1-1 / 3-2 / 5-17 / 5-21
V1.2	2024.08.02	<ol style="list-style-type: none"> <li>1. <math>V_{DDX}</math> (<math>V_{DDD}/V_{DDA}</math>): 1.2 V/1.0 V/0.9 V/0.8 V <math>\pm</math> 10%</li> <li>2. Add QFN32(4*4) PY32F072K3xU7 Pinout3, Delete QFN64 package</li> <li>3. Updated Table 5-2 / 5-4 / 5-9 / 5-11 / 5-13 / 5-20 / 5-21 / 5-25 / 5-26 / 5-27 / 5-29 / 5-39</li> <li>4. Add Table 5-32 ADC Built-in reference voltage (<math>V_{REFBUF}</math>) characteristics</li> <li>5. Add Table 5-30 LCD Controller Characteristics</li> </ol>
V1.3	2024.08.12	1. Add LQFP48 Pinout1 x7 version (105 °C) product



Puya Semiconductor Co., Ltd.

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